INCLUDE IN THIS VERSION:

COMPONENT PLACEMENT DIAGRAMS for Rev B and Rev C TC486
TC386 AND TC486 PC/104 TARGET CARD PC COMPATIBLE COMPUTERS

TECHNICAL REFERENCE MANUAL

V2.0 2 APRIL 1996

185007.C00 CP 2.4.96
All information in this manual is believed to be accurate and reliable. However, no responsibility is assumed by DSP Design Limited for its use. Since conditions of product use are outside our control, we make no warranties express or implied in relation thereto. We therefore cannot accept any liability in connection with any use of this information. Nothing herein is to be taken as a license to operate under or a recommendation to infringe any patents.

Whilst every effort has been made to ensure that this document is correct, errors can occur. If you find any errors or omissions please let us know, so that we can put this right.

All information contained in this manual is proprietary to DSP Design Limited and cannot be reproduced without the consent of DSP Design Limited. The circuit design and printed circuit board design are copyright of DSP Design Limited 1994, 1995, 1996.

DSP Design Limited
1 Apollo Studios
Charlton Kings Road
London NW5 2SB
England

Tel  (0171) 482 1773
Fax  (0171) 482 1779
## CONTENTS

1 INTRODUCTION .................................................................................................................. 1  
   1.1 OVERVIEW ............................................................................................................. 1  
   1.2 TC486 FEATURES .................................................................................................. 1  
   1.3 PC/AT COMPATIBILITY ......................................................................................... 2  
   1.4 PC/104 AS A PC EXPANSION BUS ........................................................................ 2  
   1.5 THE TC486 ARCHITECTURE ................................................................................... 2  
   1.6 GETTING STARTED QUICKLY ................................................................................ 4  

2 PROCESSOR, MEMORY AND SCATSX CHIP ........................................................................ 5  
   2.1 PROCESSOR ............................................................................................................ 5  
   2.2 SCATSX CHIP ........................................................................................................ 5  
   2.3 DRAM .................................................................................................................... 6  
   2.4 BIOS EPROM - IC12 ............................................................................................. 6  
   2.5 OPTIONS FOR THE SECOND MEMORY SOCKET - IC15 ........................................ 8  
   2.6 MEMORY ADDRESS MAP ...................................................................................... 9  

3 PERIPHERALS .................................................................................................................... 10  
   3.1 I/O ADDRESS MAP ............................................................................................... 10  
   3.2 SPEAKER ............................................................................................................... 10  
   3.3 SERIAL PORTS ....................................................................................................... 11  
   3.4 CENTRONICS PRINTER PORT .............................................................................. 11  
   3.5 CALENDAR CLOCK CHIP ..................................................................................... 12  
   3.6 FLOPPY DISK DRIVE ............................................................................................ 12  
   3.7 IDE DISK DRIVE .................................................................................................. 13  
   3.8 VGA GRAPHICS ................................................................................................... 13  
   3.9 KEYBOARD AND MOUSE ................................................................................... 13  
   3.10 UTILITY REGISTER ............................................................................................. 13  

4 PC/104 BUS AND STAND-ALONE OPERATION ..................................................................... 14  
   4.1 STAND-ALONE OPERATION .................................................................................. 14  
   4.2 PC/104 BUS ......................................................................................................... 14  
   4.3 CLOCK AND RESET SIGNALS ............................................................................. 14  
   4.4 INTERRUPTS ........................................................................................................ 15  
   4.5 DMA ..................................................................................................................... 15  

5 RESET OPTIONS .............................................................................................................. 16  
   5.1 POWER SUPPLY MONITOR ................................................................................ 16  
   5.2 ONBOARD WATCHDOG TIMER .......................................................................... 16  
   5.3 RESET SWITCH ................................................................................................... 16  
   5.4 RESETTING THE PC/104 BUS ............................................................................. 16  

6 SOFTWARE ......................................................................................................................... 17  
   6.1 BIOS ROM .......................................................................................................... 17  
   6.2 MS-DOS AND OTHER OPERATING SYSTEMS .................................................... 17  
   6.3 ROM DISK .......................................................................................................... 18  
   6.4 RAM DISK .......................................................................................................... 22  
   6.5 DISK ON CHIP .................................................................................................. 24  
   6.6 FLASH MEMORY ................................................................................................ 26  

APPENDIX A: SPECIFICATION ............................................................................................ A1  
APPENDIX B: TC486 REV B TO REV C DIFFERENCES .................................................. B1  
APPENDIX C: SET-UP PROCEDURE ............................................................................... C1  
APPENDIX D: COMPONENT PLACEMENT DIAGRAMS ................................................ D1  
APPENDIX E: TC486 OPTIONS AND ORDERING INFORMATION ............................... E1  
APPENDIX F: CABLE PIN ASSIGNMENTS ..................................................................... F1  
APPENDIX G: POWER REDUCTION OPTIONS .............................................................. G1  
APPENDIX H: FAULT REPORTING ................................................................................. H1
INTRODUCTION

1.1 OVERVIEW

To maintain our lead in advanced and highly integrated PC compatible computers, DSP Design has released an updated range of PC compatible computers all compliant with the PC/104 V2.2 specification.

These processor cards offer a range of performance options by using either the 80386SX processor or the 80486SLC processor at 25Mhz or 50Mhz. This processor board is available with a 80386SX processor running at 25Mhz (the TC386), with the 486SLC (the TC486-25) or with the 486SXLC2 internal clock doubling processor (the TC486-50) for even faster operation.

The 486SLC has an internal cache that approximately doubles throughput when compared with the 80386SX. The clock doubled 486SXLC2 further improves performance.

Where reference is made to TC486 in this document it should be noted that unless otherwise stated this refers to the TC486-25, TC486-50 and the TC386 versions of this product. Two printed circuit board revisions have been produced, the Rev B and the Rev C revisions. The Rev C revision of the TC486 has a number of enhancements over the Rev B TC486, details of which are described in APPENDIX B: DIFFERENCE BETWEEN THE REV B AND REV C TC486. Differences between the Rev B and the Rev C revisions are also described elsewhere in the manual where relevant.

The board supports up to 4M of DRAM. It also features the standard PC compatible serial ports, parallel port, keyboard interface, PS/2 mouse port and speaker controllers.

The TC486 is a single board PC/104 compatible computer that can operate as a stand-alone module or can be used in a system consisting of a number of other PC/104 modules.

A range of other PC/104 boards are available from DSP Design. Customers requiring faster processor power or more memory should consider the TC586 processor family. Contact DSP Design for up-to-date information on other products in our range.

1.2 TC486 FEATURES

- 80386SX at 25Mhz, 80486SLC at 25MHz or 80486SXLC2 clock doubled at 50MHz
- PC/104 V2.2 16-bit bus interface for wide compatibility
- COM1 and COM2 RS232 serial ports - COM2: is optionally RS485.
- Bi-directional Centronics parallel port
- Up to 4M bytes of DRAM (0k, 512k, 1M, 2M and 4M options)
- Two 32 pin sockets. One for EPROM or flash EEPROM and the other for EPROM, SRAM, Eurom DiskOnChip or flash EEPROM.
- Supports nearly 2M bytes of ROMdisk (read only disk) or DiskOnChip (read-write disk).
- Keyboard, PS/2 mouse and sound ports
- Powered by a single 5V supply
- AT compatible calendar/clock chip uses external battery
- Reset, power supply monitor and watchdog timer circuitry
1.3 PC/AT COMPATIBILITY

The TC486 offers an extremely high degree of compatibility with the IBM PC family of computers. This compatibility extends from the MS-DOS level, through BIOS-level compatibility to register-level compatibility.

The processor used on the TC486 board is supported by the Chips and Technologies SCATsx chip. The SCATsx includes on-chip peripherals - timers, interrupt controller, DMA controller etc.. These are software compatible with equivalent Intel peripheral chips used on the original IBM PC and PC/AT.

In addition to the I/O resources in the SCATsx, the chip provides other features. A calendar/clock circuit and speaker port are included, and the chip looks after clock generation, address decoding, expansion bus timing, EMS memory mapping and various other functions.

Around the SCATsx chip DSP Design has integrated a keyboard and mouse controller, two serial ports and a Centronics parallel port. These peripherals are software and hardware compatible with the IBM PC/AT.

1.4 PC/104 AS A PC EXPANSION BUS

Users can operate the TC486 as a single board computer. If expansion is required I/O boards can be accessed via the PC/104 interface provided on the TC486.

The PC/104 bus is a compact version of the IEEE P996 (PC and PC/AT) bus, optimized for embedded systems applications. DSP Design and other PC/104 manufacturers offer a wide range of I/O boards that will work with the TC486, in the same manner that a conventional PC can be enhanced by the addition of expansion boards.

The PC/104 I/O card range includes analogue and digital I/O cards, serial comms, local area network boards and other specialist functions. DSP Design manufactures a number of PC/104 modules and we are committed to expanding this range.

It is the policy of DSP Design to introduce, where appropriate, new PC/104 I/O cards which are software compatible with similar cards for the IBM PC. This has the tremendous advantage of allowing users to make use of the software that has already been written for the IBM PC cards.

1.5 THE TC486 ARCHITECTURE

The block diagram in Figure 1 shows the architecture of the TC486. The processor accesses local DRAM and EPROM memory. The SCATsx chip performs a range of house-keeping and glue logic functions, as well as providing timer, interrupt, DMA, speaker and EMS memory mapping facilities. The serial and parallel I/O chip and keyboard and mouse controller chip are connected to the internal buses.

Finally a 16-bit PC/104 interface allows the TC486 to perform memory and I/O accesses to the PC/104 bus. The SCATsx interrupt and DMA controllers are used by the on-board peripherals as well as being connected to the expansion bus.
FIGURE 1: TC486 BLOCK DIAGRAM
1.6 GETTING STARTED QUICKLY

This manual gives all of the information that most users will need in order to operate the TC486. Those people who have special requirements may require further information. If this is the case our support engineers will be pleased to help you.

DSP Design strongly recommend developing with the TCDEV development system. The TCDEV is a PC/104 based development platform. Its features include an on board VGA graphics controller with 15 pin VGA connector, a floppy and hard disk controller, a floppy drive plus cable, a small prototyping area, a full PC/AT slot for interfacing standard PC and PC/AT bus cards to the PC/104 bus and a battery for CMOS RAM backup. The TCDEV has all the standard PC connectors for interfacing to the outside world. These include two serial port 9 way D-type connectors, a parallel port 25 way D-type connector, a 5 pin DIN keyboard connector and one PS/2 style mouse connector.

DSP Design also supply the TCPSU which is a compact 30W power supply with cabling to make it easy to use with the TCDEV.

Most users will find getting started with the TC486 and TCDEV simplicity itself. The TC486 plugs directly onto the TCDEV and a short cable connects the TC486 J3 I/O socket to TCDEV I/O socket. This links the serial, parallel and keyboard etc. onto the TCDEV and in turn to the PC compatible connectors mounted on the edge of the TCDEV board.

To use your system install your DRAM in the TC486 DRAM sockets, plug the TC486 onto the TCDEV and connect the J3 I/O connector between the two boards. Connect but do not switch on the TCPSU (NOTE that this connector is polarized. Ensure that the locking tab on the power supply cable mates with the locking tab on the TCDEV connector). Connect the keyboard and VGA monitor to the appropriate connectors. Insert a bootable floppy disk into the floppy drive and switch the TCPSU on. If all is correct DOS will boot and you will be on your way.

An alternative to using floppy disks is to make use of the hard disk controller already fitted to the TCDEV. This will accept most IDE drives although the mating connector fitted to the TCDEV has been designed for the smaller 2.5 inch IDE drives. There is a suitable area reserved on the TCDEV for mounting such a drive, making this a neat solution. There are a number of 2.5 inch drives available on the market today. Please contact your supplier for more information.

Now you can explore the power of the TC486 for yourself. Users who do not have a TCDEV are advised to obtain one for development purposes. Alternatively a cable assembly will be required to mate the TC486 to the standard PC I/O connectors. Information on TC486 connectors is given in Appendix F - CABLE PIN ASSIGNMENTS.

A suitable graphics card and floppy/IDE card can be connected to the PC/104 bus for a complete target system. We recommend our TV750 and TSYST modules respectively. Please contact your supplier for more information.
2 PROCESSOR, MEMORY AND SCATsx CHIP

The TC486 single board computers contain one of three processor chips, each of which is PC compatible but which differ in their processing power. There are eight zig-zag style DRAM sockets and two sockets for EPROM devices. The standard TC486 (part number TC486-25) includes a 25MHz 80486SLC processor, 0M byte of DRAM and a 128k byte EPROM that contains the BIOS. Other options including various DRAM configurations are detailed in Appendix E: TC486 OPTIONS AND ORDERING INFORMATION.

2.1 PROCESSOR

The TC486-25 uses an 80486SLC processor running at 25MHz. The TC386 uses an 80386SX running at 25Mhz and the TC486-50 uses either the faster Texas 80486SXLC2 or the Cyrix 80486SLC2 processor running at an internal clock speed of 50Mhz. The processor is a fully CMOS chip from Intel, AMD, TI or Cyrix. The performance of the TC486 may be gauged by the processor performance ratings produced by the Norton SI program: See Table 1 below.

The TC486-50 runs much faster than the TC486-25, so is ideal for applications that require significantly greater processing power.

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>CPU TYPE</th>
<th>CPU SPEED</th>
<th>NORTON RATING (1WAIT STATE)</th>
<th>NORTON RATING (0 WAIT STATES)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TC386</td>
<td>80386SX</td>
<td>25MHz</td>
<td>21</td>
<td>23</td>
</tr>
<tr>
<td>TC486-25</td>
<td>80486SLC</td>
<td>25MHz</td>
<td>49</td>
<td>50</td>
</tr>
<tr>
<td>TC486-50</td>
<td>80486SXLC2</td>
<td>50MHz</td>
<td>85</td>
<td>88</td>
</tr>
</tbody>
</table>

TABLE 1: NORTON SI PERFORMANCE RATINGS

2.2 SCATsx CHIP

The TC486 computer is centered around the SCATsx chip from Chips and Technologies. This is a complex ASIC which provides a number of timing, control, address decoding functions and which includes a number of PC/AT compatible I/O peripheral circuits.

These peripherals are:

Two 8237 compatible DMA control units (8 channels) One 8254 compatible timer control unit (3 channels) Two 8259 compatible interrupt control unit (15 interrupts) MC146818 compatible calendar/clock and CMOS RAM chip.

The other functions provided by the SCATsx are:

- Clock generators
- Memory controller with on-board EMS registers
- Bus interfaces and conversion logic
- Peripheral I/O address decoding

The majority of the peripheral functions are the same on all IBM PC/AT compatible computers. This includes the timers, interrupt controllers and DMA controllers as well as registers such as the NMI and speaker inhibit registers, fast reset and A20 gate registers. Software which accesses the IBM PC/AT peripherals will have the same effect when running on the TC486, giving rise to a high degree of PC-compatibility.

The SCATsx chip also includes a number of internal configuration registers (ICRs). These ICRs are unique to the SCATsx chip. They control timing on the expansion bus, shadow RAM, DRAM configuration, EMS control and so forth. They are initialized by the BIOS and will not normally need to be accessed by the user.
2.3 DRAM

The main memory of the TC486 consists of Dynamic RAM (DRAM) chips. The chips used are 256Kx4 or 1Mx4 devices, which provides four possible main memory options:

- 512k bytes (using 4 256kx4 chips)
- 1M byte (using 8 256kx4 chips)
- 2M bytes (using 4 1Mx4 chips)
- 4M bytes (using 8 1Mx4 chips)

The standard configuration of the TC486 (part number TC486-25) has 0 bytes of DRAM. All DRAM kits must be ordered separately and fitted into the DRAM sockets on the PCB. See Appendix E: TC486 OPTIONS AND ORDERING INFORMATION and Appendix C: TC486 SETUP PROCEDURE for instructions on installing DRAM.

The use of sockets for the zig-zag DRAM devices means that the DRAM configuration can be altered at a later stage. DSP Design carry stock of the DRAM devices described above and are able to offer upgrades. Care must be taken when handling the TC486 and associated components. Ensure that all anti-static precautions are taken, see Appendix C - SET-UP PROCEDURE.

The DRAM is accessed using zero or one wait states. The choice of wait state depends on the processor speed and the DRAM speed. The number of wait states can be changed using the BIOS setup menu and depends on the speed of the DRAM - a 25MHz TC486 will have to use 60ns DRAM to operate without wait states. The standard BIOS is configured for one DRAM wait state. This allows 80ns DRAM to be used. A number of pre-configured BIOSes are available on the TCUTILS diskette, some with no DRAM wait states.

Note that only the first 640k bytes of DRAM are usually directly accessible by DOS. If 1M byte or more DRAM is fitted then some of the remaining DRAM is used to shadow the BIOS (see section 2.4) and the remainder can be re-mapped above the 1M byte boundary. This is achieved using the TC486 set-up utility. Any changes made to the TC486 setup will only remain valid for as long as a CMOS battery is connected and is within the required voltage limits (see section 3.5 for more information regarding battery specifications). If 2M or 4M bytes of DRAM are fitted then the DRAM beyond the 1M byte boundary can either be used as Extended or Expanded (EMS) memory.

The BIOS automatically determines the amount of DRAM present and configures internal SCATsx registers accordingly.

Memory beyond the 640k byte limit can be accessed as bank switched memory (Expanded Memory) using the EMS memory mapping circuitry provided by the SCATsx chip. This is fully documented in the SCATsx data sheet.

This mechanism is used by EMS software to access memory in excess of the 640k limit imposed by MS-DOS. EMS stands for Expanded Memory System and is a standard jointly proposed by Lotus, Intel and Microsoft (LIM). To use expanded memory the application software does not write directly to the mapping hardware, but interfaces to EMS driver software.

2.4 BIOS EPROM - IC12

When shipped from the factory, a 128k byte EPROM containing the BIOS (Basic Input Output System) is fitted in the IC12 socket. This EPROM contains machine-dependent software that is required to run an operating system. The BIOS occupies the top 64k of the 128k byte EPROM. The remaining 64k is not used in the standard configuration. See section 2.6 for more information on memory mapping of the IC12 socket.

Users who want a ROMdisk system can combine the BIOS and a ROM disk in a single EPROM or flash device fitted in the IC12 socket. This ROM disk can contain the MS-DOS operating system as well as your application program. ROMdisks are described in section 6.3.
A VGA graphics BIOS can also be programmed into the IC12 EPROM. This is not normally necessary because the VGA graphics board usually contains the VGA BIOS itself. Contact your supplier if you need further details.

IC12 is able to accept a variety of EPROM sizes: 64k, 128k, 256k, 512k and 1Mbyte devices as well as 256K and 512K byte flash devices. Since different chips have different pin assignments it is necessary to set solder links to match the type of chip installed. This is described in Appendix C: TC486 SETUP PROCEDURE.

The TC486 allows users to access large EPROMs through a small window in the 1M byte address space. DSP Design has added bank switching logic to the TC486. The high order address lines (A16-A19) of the IC12 and IC15 chips can be changed by software. The Utility Register controls these address pins (see section 3.10). ROM disk driver software uses the bank switch logic transparently to the users software. Most users will therefore not need to know the details of the operation of the bank switch logic.

The BIOS EPROM resides on an eight bit internal data bus. The SCATsx chip converts a 16-bit processor access to two eight bit accesses to the BIOS EPROM. The EPROM is accessed with several wait states. The IC12 socket accepts devices of 200ns speed or quicker.

Systems with 1Mbyte or more DRAM can use “shadow RAM” in place of the EPROM for greater speed. In this scheme the contents of the EPROM are copied by the BIOS to DRAM at the same addresses. The EPROM is then disabled and the BIOS is executed from the 16-bit wide DRAM with zero or one wait states. The video BIOS may also be shadowed. Shadowing is enabled or disabled by the setup menu. The standard BIOS uses this shadowing mechanism.
2.5 OPTIONS FOR THE SECOND MEMORY SOCKET - IC15

In many applications the IC15 socket will remain unused. Alternatively, it can be populated with EPROM, SRAM, Eurom DiskOnChip or flash devices. Since different chips have different pin assignments it is necessary to set solder links to match the type of chip installed. This is described in Appendix C: TC486 SETUP PROCEDURE. See section 2.6 for more information on memory mapping of the IC15 socket.

The IC15 socket may be fitted with one of several sizes of EPROM to provide a ROM disk. This ROM disk can be used instead of, or as well as, floppy or hard disk drives, for storing program and data files. ROM disks are described in section 6.3.

A Eurom DiskOnChip module can be installed in the IC15 socket. This provides 1M byte or 2M byte of flash memory and has a built in flash filing system, converting the module to a non-volatile read-write disk drive. Section 6.5 contains information on the DiskOnChip software.

There are certain restrictions placed on the use of the IC15 socket for the Rev B TC486 such as limited memory mapping options. Please refer to Appendix B DIFFERENCES BETWEEN REV B AND REV C TC486 for more information about these restrictions.

Alternatively, the IC15 socket can accept a 128k or 512k byte static RAM chip. This SRAM chip is mapped into the bottom 1M byte of the processor address space (see section 2.6 MEMORY MAP), so can be used as a general purpose data storage area, or it can be configured as a RAM disk. See section 6.4 for further information on RAM disks.

If an external battery is connected to the BATT pin of the J3 I/O connector, it is possible to battery back an SRAM chip in the IC15 socket, to provide a non-volatile RAM disk. The BATT pin is intended to battery backup the CMOS RAM data area in the SCATsx chip but may also be used as an alternative power source for the IC15 socket. This option is link selectable. See Appendix C - SET UP PROCEDURE.

An alternative to using an external battery is to use a battery back up socket (a "Smart Socket"). This is an IC socket which contains a small lithium battery and a circuit which switches the battery to the RAM's power supply pin when the main +5V power fails. The socket also disables the CE- pin, preventing data corruption. The part used is a Dallas Semiconductor DS1213D, which has the DSP Design part number BAT32D. Links should not be set to battery backup if a smart socket is being used.

(NOTE: The overall height of the smart socket and SRAM device will exceed the height limits of the PC/104 V2.2 specification).

A flash device (256k or 512k bytes) can be fitted into the IC15 socket. The TC486 has an onboard VPP generator for flash chips with a +12V programming voltage requirement. See section 6.6 FLASH MEMORY.

The IC15 socket accepts memory devices of 200ns or quicker.
### MEMORY ADDRESS MAP

Table 2 below shows the memory map as configured by the standard BIOS EPROM of the TC486 (185010.B**). A number of other BIOSes are available on the TCUTILS diskette. Some of these BIOSes change the memory mapping from that shown below (refer to the TCUTILS disk for more information).

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>MEMORY DEVICE DECODED</th>
<th>MEMORY SIZE</th>
</tr>
</thead>
<tbody>
<tr>
<td>FFFFF</td>
<td>BIOS EPROM (IC12)</td>
<td>64K</td>
</tr>
<tr>
<td>F0000</td>
<td>(Always the top 64k of the BIOS EPROM for all BIOSes)</td>
<td></td>
</tr>
<tr>
<td>EFFFF</td>
<td>CAN BE ALLOCATED TO PC/104 BUS OR TO THE SECOND SOCKET (IC15).</td>
<td>128K</td>
</tr>
<tr>
<td>D0000</td>
<td>(185010.B** maps this area onboard to the IC15 socket)</td>
<td></td>
</tr>
<tr>
<td>CFFFFF</td>
<td>CAN BE ALLOCATED TO PC/104 BUS OR TO THE BIOS EPROM (IC12)</td>
<td>32K</td>
</tr>
<tr>
<td>C8000</td>
<td>(185010.B** maps this area onboard to the top half of the bottom 64k of the IC12 BIOS EPROM)</td>
<td></td>
</tr>
<tr>
<td>C7FFF</td>
<td>USUALLY VGA BIOS ON PC/104 BUS. CAN BE VGA BIOS IN IC12</td>
<td>32K</td>
</tr>
<tr>
<td>C0000</td>
<td>(185010.B** maps this area onto the PC/104 bus [for VGA BIOSes])</td>
<td></td>
</tr>
<tr>
<td>BFFFFF</td>
<td>USUALLY ALLOCATED TO VGA MEMORY ON PC/104 BUS</td>
<td>128K</td>
</tr>
<tr>
<td>A0000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9FFFFF</td>
<td>DRAM (IF 1-4M OF DRAM IS FITTED)</td>
<td>128K</td>
</tr>
<tr>
<td>80000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7FFFFF</td>
<td>DRAM</td>
<td>512K</td>
</tr>
<tr>
<td>00000</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**TABLE 2: TC486 MEMORY ADDRESS MAP**
3 PERIPHERALS

This section describes the I/O address map and the on-board peripherals.

3.1 I/O ADDRESS MAP

The TC486 features a number of on-board I/O mapped resources, and supports access to the PC/104 bus I/O space as well.

All I/O mapped functions which are present on the IBM PC/AT are present at the same I/O addresses on the TC486. The TC486 is therefore compatible at the machine code or register level with the IBM PC/AT.

On-board I/O devices include registers within the SCATsx chip as well as registers in the keyboard controller, calendar/clock chip and the serial and parallel I/O chip. The on-board I/O addresses are listed in Table 3. Those addresses which are not on-board are mapped onto the PC/104 bus I/O space.

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>I/O FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>000-00F</td>
<td>DMA Controller in SCATsx</td>
</tr>
<tr>
<td>020-021</td>
<td>Interrupt unit in SCATsx</td>
</tr>
<tr>
<td>022</td>
<td>Internal Configuration Index Reg. - SCATsx</td>
</tr>
<tr>
<td>023</td>
<td>Internal Configuration Data Reg. - SCATsx</td>
</tr>
<tr>
<td>040-043</td>
<td>Timer Unit is SCATsx</td>
</tr>
<tr>
<td>061</td>
<td>Control/Status Port</td>
</tr>
<tr>
<td>062-064</td>
<td>Keyboard controller</td>
</tr>
<tr>
<td>070-071</td>
<td>Real-Time Clock</td>
</tr>
<tr>
<td>092</td>
<td>System Control Port</td>
</tr>
<tr>
<td>080-08F</td>
<td>DMA Page Registers in SCATsx</td>
</tr>
<tr>
<td>0A0-0A1</td>
<td>Interrupt Control/Status Reg. in SCATsx</td>
</tr>
<tr>
<td>0C0-0DF</td>
<td>DMA Controller in SCATsx</td>
</tr>
<tr>
<td>208-20A</td>
<td>EMS Page Registers</td>
</tr>
<tr>
<td>2F8-2FF</td>
<td>COM2: Serial Port</td>
</tr>
<tr>
<td>378-37A</td>
<td>Parallel Port</td>
</tr>
<tr>
<td>37C</td>
<td>TC486 Utility Register</td>
</tr>
<tr>
<td>3F8-3FF</td>
<td>COM1: Serial Port</td>
</tr>
</tbody>
</table>

TABLE 3: ON-BOARD I/O DEVICES

3.2 SPEAKER

A PC compatible loudspeaker port is implemented on the TC486. This allows for production of tones, tunes, keyboard clicks etc. PC software which generates sound will therefore operate as expected with the TC486. The TCDEV has a small loudspeaker mounted to it and connection is made to the TC486 via the J3 I/O cable assembly.
3.3 SERIAL PORTS

The TC486 features two RS-232 serial ports which are accessed as COM1 and COM2. Additionally the COM2 port can be configured for RS485 operation as a factory option (this option is not available on the Rev B revision of the TC486). Contact your supplier for more details. The serial ports are fully hardware and software compatible with the IBM PC/AT serial ports and all PC communications software packages will work with the serial ports. Connection is made to the serial ports via the J3 connector or if you are using a TCDEV through the standard 9 pin D-Type connectors at J4 (COM1) and J5 (COM2). These connectors are pin compatible with IBM AT computers.

The serial ports provide the full complement of RS-232 signals. Transmit Data, Request To Send (RTS) and Data Terminal Ready (DTR) are outputs from the TC486. Receive Data, Data Carrier Detect (DCD), Data Set Ready (DSR), Clear to Send (CTS) and Ring Indicator (RI) are inputs to the TC486.

Following a reset of the TC486 the COM1 serial port is initialized as 2400 baud, one stop bit, eight data bits and no parity. These parameters can be changed by the MS-DOS MODE command.

COM1 serial port uses interrupt level IRQ4 to interrupt the processor. The COM2 serial port uses interrupt level IRQ3. It should be noted that the BIOS does not make use of serial port interrupts, but that most comms software packages enable the interrupts and make use of them to increase the speed of serial data transfer. Your supplier may be able to supply interrupt driven communication packages - ask for details.

A factory fitted RS485 option is available on COM2: (Rev C revision of TC486 only). The COM2 RS485 serial port configuration provides a half duplex single twisted pair serial interface. The RS485 serial port cannot send and transmit at the same time so the direction is controlled by the RTS bit of the onboard UART. When RTS is off (inactive) the RS485 transceiver is in receive mode. This is the default state after a TC486 reset. When RTS is set active the RS485 transceiver changes to output and the TC486 can transmit. A suitable protocol needs to be agreed by all nodes on the twisted pair to ensure that only one computer transmits at any one time. No RS485 termination resistors are provided on the TC486. These must be provided externally if required.

The serial ports can be individually disabled by setting the appropriate links on the PCB (this option is not available on the Rev B revision of the TC486). The default link settings enable both serial ports. Refer to Appendix C: for details on how to disable the COM1: and COM2: serial ports. If one or both serial ports are disabled then a corresponding modification must be made to the BIOS in order to allocate the I/O address to the PC/104 bus.

Later revision C TC486 boards have a '552' type UART fitted that provides a 16 byte transmit and receive FIFO. Users of these boards can take advantage of this additional feature.

3.4 CENTRONICS PRINTER PORT

The TC486 implements a full-function Centronics compatible printer port. This port is the MS-DOS PRN device.

The Centronics port features an 8-bit data port and the full compliment of control signals - four output signals and five input signals.

The I/O signals on the printer port can be treated as general purpose digital input and output signals, and as such can be used for other applications (such as driving a small LCD display, for example).

The data port is normally used as an output port for driving a printer. It can be used as an input port however. The default setting (after reset) is output. To configure as an input the I/O select register must be written with the value 'AA' hex. To re-configure as an output write '55' hex. The I/O select register is located at I/O address 379 hex.
The Centronics port signals are brought out on the J3 I/O connector on the TC486. On the TCDEV the parallel port is accessed via a PC compatible 25 way female D-type connector.

The parallel port uses interrupt IRQ7 to interrupt the processor. Optionally this can be allocated to the PC/104 bus (this option is not available on the Rev B revision of the TC486). Refer to Appendix C: for information on how to allocate IRQ7 to the PC/104 bus.

Additionally the parallel port can be disabled by setting the appropriate link on the PCB (this option is not available on the Rev B revision of the TC486). If the parallel port is disabled then a corresponding modification must be made to the BIOS in order to allocate the I/O address to the PC/104 bus. Refer to Appendix C: for details on how to disable the LPT1: parallel port.

3.5 CALENDAR CLOCK CHIP

Calendar/clock functions are implemented within the SCATsx chip. These functions emulate those found in the Motorola MC146818 chip. This chip provides time of day functions, calendar functions and CMOS RAM for storing setup parameters. An alarm facility is also provided; this allows an interrupt to be generated when a particular time is reached.

The calendar/clock chip may be accessed through the MS-DOS calls (interrupt 1AH) or with MS-DOS TIME and DATE commands. As well as the calendar clock functions there are 114 bytes of static RAM which are backed up by the battery. This is used to store configuration parameters used by the BIOS.

A battery can be used to provide power to maintain the clock and CMOS RAM when the main power is not present. This external battery should be connected between the BATT input and GND of J3. The battery voltage should be between 3.6V and 5V and can be either be a rechargeable battery (e.g. Nicad) or a non-rechargeable battery (e.g. Lithium).

The SCATsx chip draws approx. 10uA from the battery when the TC486 is powered down and draws no current when operating normally (i.e. powered up).

The TCDEV has a 3.6V 100mAhr Nicad rechargeable battery installed. This connects to the BATT input via an enable/disable jumper, as described in the TCDEV manual. It is estimated that the TCDEV Nicad battery should be sufficient for the clock to operate for several months in the absence of the +5V power supply. The jumper E2 is provided on the TCDEV which can be used to disconnect the battery in order to extend the battery life. The battery should be disconnected while the TC486/TCDEV is in storage.

NOTE: The circuit shown above is identical to the circuit used on the TCDEV. This circuit is suitable only when using a Nicad battery of the type used on the TCDEV. The circuit shown in figure 2 is not suitable for Lithium or other battery types.

3.6 FLOPPY DISK DRIVE

Users who require a floppy drive can use the TCDEV or TSYST boards manufactured by DSP Design. The TCDEV incorporates a complete floppy system, including a floppy diskette drive and cable. Connection to the TC486 is via the PC/104 bus.
3.7 IDE DISK DRIVE

Users who require an IDE hard drive can use the TCDEV or TSYST boards manufactured by DSP Design.

The TCDEV incorporates an IDE controller and standard 2.5 inch IDE drive connector. Your supplier can supply 2.5” IDE disk drives. These can be mounted to the TCDEV to give a complete hard disk solution. A 2.5 inch to 3.5 inch IDE drive converter cable is available which allows 3.5 inch hard disk drives to be connected to the TCDEV (a separate PSU is required for the 3.5 inch drive in this configuration). The converter cable is called the IDE3020.

The TSYST board accepts 3.5 inch hard drives as standard and can be interfaced to a 2.5 inch drive using the IDE3020 cable assembly.

3.8 VGA GRAPHICS

Users who require VGA graphics can use the TCDEV or TV750 boards manufactured by DSP Design. The TCDEV incorporates a simple VGA system including a standard 15 pin VGA connector for easy connection to VGA monitors. Connection to the TC486 is via the PC/104 bus.

The TV750 is a PC/104 format board and is a high performance VGA controller available with up to 1Mbyte of video memory. It can drive CRT displays and a wide range of flat panels including passive STN and active-matrix TFT LCDs, EL and plasma panels.

3.9 KEYBOARD AND MOUSE

The TC486 uses an AT type keyboard, as opposed to the XT type. Many keyboards operate in both modes and have a switch to select PC/XT or AT operation. Your supplier can provide a suitable keyboard.

In many applications the familiar desktop keyboard is inappropriate. A variety of industrial keyboards and keypads are available - contact your dealer or DSP Design for details. DSP Design suggest that you avoid the keypad encoders from Keymat Technologies as we have had problems with noise with these keyboard encoders. The TC486 will work without a keyboard if required.

Users should avoid plugging in the keyboard when the TC486 is powered on.

The keyboard controller chip on the TC486 also includes a PS/2 style mouse port.

Connections to the keyboard and mouse are made through the J3 connector or if using the TCDEV through the J8 mouse port connector (PS/2 style) and the J7 AT keyboard connector.

3.10 UTILITY REGISTER

The TC486 has a Utility Register which controls a number of peripheral functions including the watchdog and Vpp generator and EPROM bank switching. These resources appear in the I/O address space. The Utility Register is an 8 bit write only register at address 37CH. Bits 0-3 and 6 are used for bank switching for the IC12 and IC15 sockets. Bits 4 and 5 are used to control the watchdog timer. Bit 7 is used to control the onboard vpp voltage generator. The Utility Register is reset following a hardware reset of the TC486.

The utility register is used extensively by DSP Design’s ROM disk driver software and flash programming utility and will not normally be accessed by the user except perhaps for watchdog timer programming.

Example programs on the Utility Disk show how to use the watchdog timer and Vpp generator functions of the utility register.
4 PC/104 BUS AND STAND-ALONE OPERATION

The TC486 will operate as a stand alone single board computer, or can use the PC/104 bus interface to expand its capabilities with the wide range of PC/104 bus I/O cards currently available. This section of the manual describes first the stand alone operation and then operation on the PC/104 bus.

4.1 STAND-ALONE OPERATION

The TC486 will operate as a single board computer with the addition of the appropriate peripherals (keyboard, monitor etc.) and a single +5V power supply. In stand-alone operation the TC486 need not be plugged into a bus.

The TC486 requires a +5V power supply. Power can be supplied in one of two ways.

The PC/104 bus connectors have various +5V and GND pins available. See Appendix F for actual pin numbers. These pins can be grouped and the resulting +5V and GND connected to the power supply. The second and by far the most convenient option is to use the alternate power connector J4. This is a four pin right-angle Molex socket. +5V and GND should be connected to J4 using a suitable mating connector. See Appendix F: for pin assignments and part numbers.

4.2 PC/104 BUS

The TC486 is PC/104 compliant. That is, the TC486 conforms to both the electrical and mechanical specifications laid down by the PC/104 V2.2 document.

The TC486 is able to interface with both the 8-bit and 16-bit modules that meet the PC/104 specification.

The TC486 has been built around the PC/104 V2.2 specification. This includes the use of polarizing pins on the J1 & J2 connectors. Some earlier versions of the PC/104 specification did not use polarizing pins and it was seen that this could result in possible mis-alignment and subsequent product failure if power was applied before the error was discovered. ‘KEY’ positions have been assigned to the J1 and J2 connectors. These can be seen on the J1 and J2 pin assignment diagrams detailed in Appendix F: The ‘KEY’ positions have had their ‘pin’ removed and the socket hole has been blocked to prevent entry by any adjacent pin.

Users should note that any boards produced to an earlier PC/104 specification will not mate with V2.2 boards. However it is quite simple to modify the J1 and J2 connectors to circumvent this problem. Prior to the V2.2 specification J2 could have been a right angled connector. The V2.2 specification does not allow this and so both J1 and J2 on the TC486 are mounted vertically.

10K ohm pull up resistors have been added to the SD0 - SD15, DREQ0 - DREQ7, /IOCHCHK and all IRQ signals on the PC/104 bus. The IOCHRDY, /IOCS16, /MEMCS16 and /ZEROWS signals have 330 ohm pull up resistors on the PC/104 bus.

4.3 CLOCK AND RESET SIGNALS

Two PC/104 clocks are provided: the bus clock (BUSCLK) and an asynchronous oscillator (OSC). The OSC signal is a clock running at 14.3181MHz. The PC bus clock normally runs at one third of the processor clock [8.33 MHz], but can be altered by using the TC486 BIOS setup utility.

The TC486 can reset the PC/104 bus. See section 5 for details. The TC486 drives the PC bus RESETDRV signal but cannot be reset by the RESETDRV signal.

The TC486 can be reset by issuing a low going pulse on the /RESET line of the J3 connector. The TC486 will then force the RESETDRV signal of the PC/104 bus to be driven. In this way a system reset can be generated by an external signal or switch. The TCDEV has a push button
switch connected between /RESET and GND. Pressing this switch momentarily will reset the system.

4.4 INTERRUPTS

The following interrupt signals are connected directly from the PC/104 bus to the SCATsx chip: IRQ9 (IRQ2), IRQ3 to IRQ6, IRQ10, IRQ11, IRQ14, IRQ15 and IOCHCK-. If any interrupts are used by the on-board peripherals then they are not available for use by a PC/104 bus card. IRQ7 is normally allocated to the printer port. Refer to Appendix C for details of how to allocate IRQ7 to the PC/104 bus (this option is not available on the Rev B TC486).

4.5 DMA

The following DMA signals are available on the PC/104 bus. DREQ0 - DREQ3 & /DACK0 - /DACK3 are used for eight bit transfers. DREQ5 - DREQ7 & /DACK5 - /DACK7 are used for 16 bit transfers. The bus master facility (using the /MASTER signal) is not supported on the TC486.
5 RESET OPTIONS

A full set of reset options exist for the TC486. The reset circuit is built around the Maxim MAX691 chip. This chip includes a power supply monitor and a watchdog timer. To avoid glitches on the reset signal the MAX691 will always hold the reset signal asserted for a minimum of 200ms. This ensures all circuitry is properly reset, and conforms to the PC bus specification.

The MAX691 resets the SCATsx chip, which in turn resets the PC/104 bus by driving the RESETDRV signal high.

5.1 POWER SUPPLY MONITOR

The MAX691 monitors the +5V supply voltage. When the supply drops below about 4.65V the MAX691 will assert the TC486 reset signal. Once the power supply returns to being within specification, the reset signal will be released after 200ms. This circuit prevents power "brown-out" causing unpredictable behavior.

Users should note that if the voltage drop across the cables which link the power supply to the TC486 is excessive then the power supply monitor may reset the TC486. This may also happen if there are noise spikes on the power supply. It is recommended that all power supply cables be as thick and short as possible to minimize the voltage drop across them.

5.2 ONBOARD WATCHDOG TIMER

A watchdog timer exists on the MAX691. The function of a watchdog timer is to reset a computer if the software has crashed. The correct operation of the timer relies on software to access the watchdog timer hardware on a regular basis. If the software crashes, the watchdog timer will not be "kicked" and so eventually it will time-out and reset the computer. The watchdog timer function is accessed via the on-board Utility Register at I/O 37Ch.

The Utility Register is a multi-function register which among other things gives access to the watchdog pin on the MAX691. After power-up or a system hardware reset this function is disabled. The watchdog is enabled by driving this pin either high or low for a minimum of 1s (70ms for Rev B TC486). Once this has been initiated, an internal clock to the MAX691 starts counting and will continue to count until a change in polarity on the watchdog input or until the input is disabled. If the clock is allowed to count for 1 second, (70ms for the Rev B TC486), the MAX691 will timeout and issue a system reset. To stop this happening, the watchdog input pin needs to be toggled at least once every 1 second (every 70ms for the Rev B TC486). The TCUTILS utility disk has documented sample code illustrating the use of the watchdog function.

5.3 RESET SWITCH

A reset switch or similar can be connected to the TC486 via the J3 I/O connector. The reset switch connects between J3 pins 23 & 24 (pin 24 is the /RESET input. Pin 23 is a GND pin). See section 4.3 for more details.

5.4 RESETTING THE PC/104 BUS

The TC486 always resets the PC/104 bus via the RESETDRV signal. The active high RESETDRV signal is asserted whenever the MAX691 is driving the TC486 on-board reset signal - that is, in response to a power failure, watchdog timer time-out, or a low going pulse on the /RESET line of the J3 I/O connector.

It is not possible to reset the TC486 by driving the RESETDRV signal on the PC/104 bus.
6 SOFTWARE

The TC486 offers a very high degree of PC compatibility. The vast majority of software (both operating systems and applications software) which will run on IBM PC/AT will also run satisfactorily on the TC486.

Most users will wish to use the MS-DOS operating system (booting from a hard disk, floppy disk or ROM-disk) and then run off the shelf software, or their own application. DSP Design offers a number of software products to ease software development.

6.1 BIOS ROM

The BIOS is a program which interfaces between the TC486 hardware, the operating system and application code. It is responsible for controlling the TC486 hardware and providing a standard interface to the higher levels of software. The BIOS also deals with functions such as initialization and testing the TC486 hardware following power-on.

The TC486 uses a BIOS supplied by Chips & Technologies. The BIOS is stored in the top 64k of a 128k byte EPROM, which is plugged into the IC12 socket. Users should note that the BIOS is the copyright of Chips & Technologies.

Under some circumstances the TC486 BIOS may need to be modified or additional BIOS code may need to be added to the BIOS EPROM. Tools exist to deal with these issues, so contact your dealer for details. A number of pre-configured BIOSes are available on the TCUTILS diskette.

6.2 MS-DOS AND OTHER OPERATING SYSTEMS

The TC486 will run any version of MS-DOS. The computer will boot MS-DOS from a floppy disk, from a hard disk or from a ROM disk.

DSP Design supply Microsoft's MS-DOS operating system. Users should note that most copies of MS-DOS obtained from other sources may not legally be run on the TC486 under the terms of the Microsoft license agreement. Bootleg copies of the operating system of course may not be run on the TC486.

A floppy disk containing MS-DOS can be programmed into an EPROM, which is referred to as a "ROM disk". Conceptually the ROM disk is the same as a read-only floppy disk - it can be used to store programs and data files as well as the operating system. Following power-on the TC486 will load the operating system from the EPROM, and with a suitable AUTOEXEC.BAT file the user's application program will then be loaded and executed.

Any other operating system which will run on a 386 or 486 based desk top computer should also run on the TC486. For example Windows has been successfully tested on the TC486.
6.3 ROM DISK

6.3.1 INTRODUCTION

The ability to operate without mechanical disk drives is a key feature of the TC486. To do this you can copy a floppy disk into EPROMs which appear to the TC486 user as read-only disk drives. These EPROMs are called ROM disks. As well as being more robust than mechanical drives they are also very much faster.

ROM disks are inherently read only devices. A ROM disk is created by taking an exact image of a floppy disk and transferring the data into an EPROM using an EPROM programmer. A ROM disk driver then allows this EPROM image to behave as a logical disk drive.

A number of ROM disk options exist for TC386/486 users:

1. Combine the system BIOS, ROM disk driver, MS-DOS and user files in a single ROM disk in the IC12 socket (using a 256k byte or bigger EPROM).
2. Install a single ROM disk in the IC15 socket.
3. Install ROM disks in both IC12 and IC15 to provide two ROM disks.

For small ROM disk applications the first option is recommended. The BIOS can be combined with the MS-DOS operating system the users application code and the ROM disk driver and be blown into a single 256k, 512k, or 1M byte EPROM in the IC12 socket.

The second option allows a ROM disk to be fitted in the IC15 socket while the IC12 EPROM contains the BIOS and the ROM disk driver. The IC15 ROM disk can be used with or without the combined BIOS and MS-DOS ROM disk in the IC12 socket.

The third option combines the first and second options together creating two ROM disks, one in the IC12 socket and one in the IC15 socket

6.3.2 GENERATING A ROM DISK IMAGE FILE

Using the software provided on the TCUTILS utility diskette and following the instructions below you will be able to create a ROM disk for running your ‘diskless’ application.

CREATE A FLOPPY CONTAINING YOUR FILES

Copy the files you want on your ROM disk onto a freshly formatted floppy disk. ALWAYS format your disk with the /U option to ensure that the disk is not fragmented. If you want to boot MS-DOS from your ROM disk format the disk using the /S option as well, to copy the MS-DOS system files onto the disk.

Use a 360k or 720k disk format if possible since less space is allocated on smaller disks for directories and file allocation tables.

Once your disk has been formatted you should not erase any files as this will fragment the data on your disk.

There is one exception to this rule. If you are using MS-DOS 6.x then the DBLSPACE.BIN will probably have to be removed, or else it will take an unacceptably large amount of the ROM disk capacity. To do this, format the floppy with the /S and /U options (do not try to add DOS after formatting with the SYS command). Then make the DBLSPACE.BIN visible by typing ’ATTRIB *.BIN -H’. Finally erase the DBLSPACE.BIN file.

To check that the data on your disk will fit into your EPROM run the MS-DOS CHKDSK program. The EPROM space required for the ROMdisk image is approximately the difference between the ’total disk space’ and the number of ’bytes available on disk’. If the space required is larger
than the available space then choose a larger EPROM, use a second ROM disk or start again
with smaller files.

Now copy your program and data files to the floppy disk. If you want your application to run
immediately after DOS has booted you will be required to make the appropriate entry in your
AUTOEXEC.BAT file.

Now move the write protect tab on your floppy to write protect your disk and check that it
performs as expected in your development system.

**MAKING A BINARY IMAGE**

Using Table 4 select your ROM disk configuration:

<table>
<thead>
<tr>
<th>ROM disk size (bytes)</th>
<th>EPROM size (bytes)</th>
<th>EPROM socket</th>
<th>MSDOSVOL /K PARAMETER</th>
</tr>
</thead>
<tbody>
<tr>
<td>1M</td>
<td>1M</td>
<td>IC15</td>
<td>/K:400</td>
</tr>
<tr>
<td>956k</td>
<td>1M</td>
<td>IC12</td>
<td>/K:3BC</td>
</tr>
<tr>
<td>512k</td>
<td>512k</td>
<td>IC15</td>
<td>/K:200</td>
</tr>
<tr>
<td>444k</td>
<td>512k</td>
<td>IC12</td>
<td>/K:1BC</td>
</tr>
<tr>
<td>256k</td>
<td>256k</td>
<td>IC15</td>
<td>/K:100</td>
</tr>
<tr>
<td>188k</td>
<td>256k</td>
<td>IC12</td>
<td>/K:BC</td>
</tr>
</tbody>
</table>

**TABLE 4: ROMDISK SIZE OPTIONS**

For example, examining a 720k byte floppy disk with CHKDSK reveals a total disk space of
730,112 bytes and bytes available on disk of 546,816 bytes. The difference is (approximately)
the ROM disk size of 183,286 bytes. This is approximately 180k bytes.

The table above indicates that this example ROM disk should fit in any of the configurations. The
smallest option (188k maximum ROM disk size) may seem optimal. However depending on the
structure of your floppy disk it may not fit. The next option (a 256k byte EPROM in IC15) will be
adequate, but remember that IC15 is often used as a RAM disk socket (in fact, this is the default
configuration for IC15), and you will still need an EPROM in IC12 containing the BIOS and ROM
disk driver. So the next option, a 512k byte EPROM in IC12, may turn out to be most convenient:
it is certainly large enough, and it leaves IC15 available for a RAM disk if required.

Assuming that you have selected a 512k byte EPROM in IC12 you may now create a file which is
an image of the floppy disk by using the MKDOSVOL program. Using a hard disk based system,
place your ROM disk floppy in drive A: and at the C: prompt type:

**MKDOSVOL IMAGE /K:1BC**

The MKDOSVOL utility is available on the TCUTILS Utility Disk.

This will create a binary image of the floppy in a file on your hard disk called IMAGE. Select your
/K parameter from the table above depending on your ROM disk size.

The /K: switch instructs the program how many kilobytes to copy to the file IMAGE. The 1BC is
the number of kilobytes in HEXADECIMAL (=444k bytes). Note that MKDOSVOL creates a file
consisting of an integral number of floppy disk tracks, so the file IMAGE may be somewhat larger
than you expect.

To ensure that your ROM disk really fits you should view the end of the IMAGE file. At the end of
the IMAGE file you should see a block of at least 256 bytes of 0F6H. This is the pattern which
the floppy disk format program uses to fill unused space on floppy disks.
BREAKING THE IMAGE INTO SMALLER FILES

If you prefer to deal with smaller files then you may use the FB64 program to break the IMAGE file into smaller 64k byte files.

Example:

FB64 IMAGE

This will create a sequence of 64k byte files called IMAGE.001, IMAGE.002 etc..

The FB64 utility can be found on the TCUTILS Utility Diskette.

6.3.3 CHOOSING A DRIVER

Before blowing the EPROMs you will need to select the ROM disk driver (from the TCUTILS Utility Disk), to match your system configuration. The ROM disk drivers differ in the way that they allocate the drive letters (A:, B:, C: etc.) between the ROM disks and floppy disks.

The ROM disk driver filename is in the format TC4_xyz_.DRV where x, y and z specify the MS-DOS logical drive letters assigned to the IC12 ROM disk, the IC15 ROM disk and floppy drive(0) respectively.

Example:

TC_BAC_.DRV

This ROM disk driver maps the IC12 ROM disk onto drive B:, the IC15 ROM disk onto drive A: and floppy drive(0) onto drive C:.

Each driver has a default and alternate drive allocation table. The alternate drive table is sometimes useful during system debugging. It can be selected by pressing 'T' when prompted during the boot process.

Select a ROM disk driver from Table 4 to match your system requirements.

<table>
<thead>
<tr>
<th>DRIVER</th>
<th>A:</th>
<th>B:</th>
<th>C:</th>
<th>alt A:</th>
<th>alt B:</th>
<th>alt C:</th>
</tr>
</thead>
<tbody>
<tr>
<td>TC4_ABC_.DRV</td>
<td>IC12</td>
<td>IC15</td>
<td>FLOPPY</td>
<td>FLOPPY</td>
<td>IC15</td>
<td>IC12</td>
</tr>
<tr>
<td>TC4_BAC_.DRV</td>
<td>IC15</td>
<td>IC12</td>
<td>FLOPPY</td>
<td>FLOPPY</td>
<td>IC12</td>
<td>IC15</td>
</tr>
<tr>
<td>TC4_BCA_.DRV</td>
<td>FLOPPY</td>
<td>IC12</td>
<td>IC15</td>
<td>IC12</td>
<td>IC15</td>
<td>FLOPPY</td>
</tr>
<tr>
<td>TC4_AB__.DRV</td>
<td>IC12</td>
<td>IC15</td>
<td>none</td>
<td>IC15</td>
<td>IC12</td>
<td>none</td>
</tr>
</tbody>
</table>

TABLE 5: ROMDISK DRIVER OPTIONS

6.3.4 ASSEMBLING THE COMPONENTS AND PROGRAMMING AN EPROM

You now have the elements that you need to assemble a ROM disk. These elements need to be assembled in the correct order and programmed into 200ns or faster EPROM or EPROMs.

Program the disk image (in the file called IMAGE) into your EPROM starting at address 00000h.
If you are programming an EPROM for IC12 then the system BIOS must be copied from the top 64k of your TC486 BIOS EPROM into the top 64k of the new EPROM. The system BIOS is located at address 10000h in a 128k EPROM (as shipped with the TC486), 30000h in a 256k byte EPROM, 70000h in a 512k byte EPROM and address F0000h in a 1M byte EPROM.

Your ROM disk driver must be programmed into the IC12 EPROM at address F000h in a 128k byte EPROM, address 2F000h in a 256k byte EPROM, address 6F000h in a 512k byte EPROM or DF000h in a 1M byte EPROM. If you are programming a ROM disk for IC15 then you still need to program the ROM disk driver into the IC12 EPROM.

The ROM disk drivers are BIOS extensions ROMs. This is a program which is found during the BIOS ROM search process shortly after reset. It must appear in the logical address space in the address range C8000H to EFFFFH on a 4k byte boundary. The instructions above ensure the ROM disk driver is located at logical address CF000h.

### 6.3.5 USING THE ROM DISK

When the ROM disk EPROM(s) have been blown they are simply plugged into the appropriate sockets on the TC386/486 and the computer is powered on. Ensure that you have set the correct link positions for the size of EPROM that you are using (see Appendix C SET-UP PROCEDURE for information regarding link positions).

The ROM disk driver will display a sign on message to confirm that it has been located and it will invite you to type a key to select the alternate disk drive allocation. If the correct key is not pressed within a few seconds of this message being displayed then the default drive allocation is chosen and the booting process proceeds.

If an IDE drive is included in the system this will always be drive C: regardless of the ROM disk configuration. The ROM disk drive C: allocation will move to the next free drive i.e. D:. If two IDE drives are being used then the ROMdisk will move to E:. Systems without an IDE drive will always boot from the A: disk (which can be floppy or ROM disk). Systems with an IDE drive will boot from A: or C: (IDE drive) depending on the boot drive option set in the BIOS setup menu (default is A: then C:).

The ROM disk driver maps 64k byte blocks of the ROM disk EPROM into address E000:0 during each ROM disk access. It should be noted that any modules present on the bus at these addresses will see /MEMRD signals during ROM disk access. It is recommended that addresses E000:0 to EFFFF:F are not allocated to bus devices when using ROM disks.

### 6.3.6 FLASH MEMORY DEVICES AS ROM DISKS.

It is possible to install flash memory chips in either or both of the IC12 and IC15 sockets, and to use them as ROM disks.

Additionally a flash device installed in the IC15 socket can be re-programmed on-board using the flash programming utilities provided on the TCUTILS utility diskette.

This will allow the IC15 ROM disk to be erased and re-programmed without removing the flash chip from the TC486 IC15 socket. This could be of use in applications where particular files need to be updated from time to time. See section 6.6 for more details on flash memory.

If you are using a 29F040 flash device as a ROMdisk and are programming the flash device off-board (not using any of the flash programming utilities provided on the TCUTILS diskette), you will be required to program the first 256k byte of the ROMdisk image into the top half of the 28F040 device and the last 256k byte of the ROMdisk image into the bottom half of the 28F040 device.
6.4 RAM DISK

RAM disks can also be implemented on the TC486. These are similar in concept to ROM disks except that, being implemented in RAM, they are read-write disks rather than read-only disks. A further difference is that the ROM disk driver is effectively an extension to the BIOS, while the RAM disk driver is a loadable device driver, loaded from disk by MS-DOS.

(Users will note that RAM disk drivers are also provided in MS-DOS by Microsoft. These RAM disk drivers make use of the DRAM memory, and data stored in these RAM disks is lost when the computer is reset. DSP Design's RAM disks are for use on non-volatile Static RAM).

DSP Design's RAM disk driver implements the RAM disk in the IC15 socket. A 128K byte or 512K byte SRAM chip can be installed in the IC15 socket.

The RAM disk driver is supplied as a loadable device driver, rather than being stored in EPROM like the ROM disk drivers. An entry is made in the CONFIG.SYS file if RAM disks are to be used.

The DSP Design static RAM disk driver takes the form of a loadable device driver, called TCRAM.SYS. The device driver is a file that is placed in the root directory of the boot disk and which is invoked by a command in the CONFIG.SYS file. The driver program is provided on the TC486 Utilities Disk, part number TCUTILS.

There are two files associated with DSP Design's RAM Disk - the driver itself, called TCRAM.SYS, and a formatting and status program called TCRAM.EXE.

The driver is installed in the CONFIG.SYS file as an entry in the following form:

```
DEVICE=TCRAM.SYS /O=xxxx /S=xxxx
```

Where /O indicates the starting page Offset of the RAM disk and /S is the number of 512K byte Sectors (in hex) that the RAM disk will occupy.

For a 128K SRAM use: DEVICE=TCRAM.SYS /O=0002 /S=0100

For a 512K SRAM use: DEVICE=TCRAM.SYS /O=0000 /S=0400

The settings shown above will not normally need to be changed for the device types indicated.

The TCRAM.EXE program can be run from the MS-DOS command line. It allows the user to format the RAM disks, and can also report on the size and status of RAM disks. It can be run in four ways. Use:

```
TCRAM       to display status of all RAM disk drives
TCRAM d:    to display status of RAM disk drive d:
TCRAM d:/F  to format RAM disk drive d:
TCRAM d:/F /P to format drive d: with parameters (not usually used - the program will prompt you for various parameters).
```

The status reported by TCRAM.EXE is the size of the RAM disk and whether or not it is formatted. The format options ask whether you are sure you want to format the disk, and if so the disk is formatted ready to accept new data. All files previously stored on the disk will be erased.

Examples of using the TCRAM.EXE program are:

```
TCRAM C:    this will report on the size of RAM disk drive C:
TCRAM C:/F  this will format the RAM disk drive C:
```

Both the TCRAM.SYS driver and the TCRAM.EXE program produce a number of self-explanatory status messages.
All MS-DOS functions that work on floppy and hard disks will behave as expected with RAM disks (with the exception of formatting commands). In particular the CHKDSK command can be used to display information about the number of files etc. Similarly subdirectories can be created on the RAM disks, and files can be protected and hidden using normal DOS commands.

The second socket (IC15) can be battery backed as discussed in section 2.5: OPTIONS FOR THE SECOND MEMORY SOCKET - IC15. Refer to this section for details and to Appendix C: SETUP PROCEDURE.
6.5 DISK ON CHIP

The TC486 is capable of being used with Eurom DiskOnChip devices. These are flash devices with their own flash file system programmed into the flash chip by DSP Design.

The DiskOnChip product from Eurom makes it easy to add a moderately sized read-write solid state disk to the TC486 range of processor modules. Disks of about 1M byte and 2Mbytes can be used (it may be that larger parts will become available later).

The DiskOnChip is a 28-pin module which is installed in the IC15 position on the TC486. The module contains 1M or 2M bytes of Flash memory, a programming voltage source and an ASIC which controls the other elements of the DiskOnChip module.

The effect of the DiskOnChip and its flash file system is to give the user a read-write disk drive, which can be used to boot MS-DOS from, and to store programs and/or data. The flash file system requires no additional device drivers or drive redirecting drivers (unlike the Microsoft FFS). It operates as an INT13 device, and so all DOS utilities which work with hard disk drives (such as FDISK, FORMAT, CHKDSK etc.) will work properly.

The DiskOnChip is usually allocated drive C:. However other disks in the system may have an effect upon the DiskOnChip drive letter allocation. Read the README.ROM file in the ROMDISK directory on the TCUTILS Utility Disk for more information on drive letter allocation.

6.5.1 SELECTING AND INSTALLING THE DISK ON CHIP MODULE.

There are currently two sizes of DiskOnChip modules available. The 1Mbyte version yields approx 790k of usable read-write disk space. The 2M byte version yields approx 1.8M bytes.

The Eurom DiskOnChip module is a 28 pin DIP device that plugs into the IC15 position on the TC486. Pin 1 of the DiskOnChip must be plugged into pin 3 on the IC15 socket. That is, the 28 pin device resides in the lower section of the 32 pin IC15 socket.

The DiskOnChip modules flash file system is pre-programmed into the DiskOnChip module by DSP Design prior to shipping.

The TC486 must be configured for the DiskOnChip module by setting various link positions on the rear of the TC486. Refer to Appendix C: SET-UP PROCEDURE for TC486 and DiskOnChip configuration information.

6.5.2 PROGRAMMING THE BIOS EPROM.

To support the DiskOnChip it is necessary to select a suitable BIOS for the IC12 EPROM and also to add a BIOS extension in IC12, which ensures the DiskOnChip is properly initialized at reset.

The TC486 BIOS must configure addresses D000:0 to DFFF:F and C800:0 to CFFF:F to be onboard addresses for the DiskOnChip to work. Suitable BIOSes has been created for this purpose (185015.B** and 185016.B**) and are available on the TCUTILS Utility Disk.

The DiskOnChip reset BIOS extension called DOCRESET.DRV, is to be programmed into the BIOS EPROM at address C800:0.

STEP BY STEP EPROM PROGRAMMING INSTRUCTIONS.
i) Load the 185015.B** or 185016.B** TC486 BIOS image into the EPROM programmer, 64k from the top of the EPROM, at offset 10000h in a 27C1001 (128K byte) EPROM, at offset 30000h in a 27C2001 (256K byte) EPROM, at offset 70000h in a 27C4001 (512K byte) EPROM or at offset F0000h in a 27C080 (1M byte) EPROM.

ii) Load the reset BIOS extension (DOCRESET.DRV), into the EPROM programmer at offset 08000h in a 27C1001 (128K byte) EPROM, at offset 28000h in a 27C2001 (256K byte) EPROM, at offset 68000h in a 27C4001 (512k byte) EPROM or at offset E8000h in a 28C080 (1M byte) EPROM.

iii) If using 185016.B** load the VGA BIOS image that you have chosen into the EPROM programmer at BIOS EPROM offset 00000 in a 27C1001 (128K byte) EPROM, at offset 20000h in a 27C2001 (256K byte) EPROM, at 60000h in a 27C4001 (512K byte) EPROM or at E0000h in a 27C080 (1M byte) EPROM.

iv) Program the EPROM.

Install the BIOS EPROM into the IC12 socket on the TC486.

NOTE: When using a DiskOnChip module with the Rev B TC486 that IC12 must be a 128k byte EPROM.

6.5.3 USING THE DISK ON CHIP MODULE FOR THE FIRST TIME.

The first time the DiskOnChip module is used it will perform a low level format of itself automatically and will then require partitioning and formatting identical to that required on a new hard disk drive.

To partition the DiskOnChip disk you must run the MS-DOS 'FDISK' program in the usual way. This will involve creating an active primary DOS partition. Following this you will be required to re-boot and then format the disk.

To format the disk use the MS-DOS 'FORMAT' command. If you want the disk to be bootable use the 'format c:/s /u' command to place the operating system onto the disk and to make it bootable.

The DiskOnChip module will now behave in the same way as a hard disk drive. You will not be required to partition or format the disk again unless you choose to do so.

*NOTE

MSDOS V6.22 has problems FDISKing the Eurom DiskOnChip device. If you encounter this problem you may be required to FDISK with an earlier version of MSDOS (e.g. V6.20) and then format the DiskOnChip with MSDOS V6.22.
6.6 FLASH MEMORY

The TC486 is able to accept a variety of Flash memory chips in the IC12 and IC15 sockets. The TCUTILS Utility Disk contains the necessary software for the programming flash chips in the IC15 socket so that they can be used as ROM disks.

6.6.1 INTRODUCTION

A flash programming utility provides facilities for programming data into an Intel or AMD 28F020 256k or 29F040 512k byte flash EEPROM memory chip fitted in the second socket (IC15) on the TC386/486. The program writes an MS-DOS file that could be on a ROM, RAM or floppy disk into the flash device at a specified offset.

The flash programming utility is normally used to write a floppy disk image to the flash EEPROM for use by a ROM disk driver.

Because of the nature of the 28F020 flash device, if data is to be rewritten the whole device must be erased first. The TC28F020.EXE programming utility is used to program the 28F020 device in the IC15 socket and is available on the TCUTILS utility diskette.

The 29F040 contains eight 64k byte sectors which can be erased and programmed separately. The TC29F040.EXE flash programming utility is used to program 29F040 flash devices in the IC15 socket and is available on the TCUTILS utility diskette.

6.6.2 PROGRAMMING A 28F020 FLASH DEVICE.

The program which programs the 28F020 flash device is called TC28F020.EXE. It is run with the following parameters:

```
TC28F020 -e -p<filename> -oxxxxx -lxxxxx -q
```

-e If -e is specified the entire device will be erased. If -e is not specified the device will not be erased. The default is to not erase.

-p -p<filename> program the specified file into the device. This parameter defaults to "DO NOT PROGRAM".

-o -oxxxxx. Start programming the file at this offset from the start of the flash device. xxxxx is a 20 bit hexadecimal number. This parameter defaults to 0.

-l -lxxxxx. This is the maximum amount of data to program into the flash EEPROM. The number of bytes programmed will be the either the file length or the number of bytes specified by this parameter whichever is the smaller. This parameter defaults to 3ffff bytes which is the size of the 28F020 device.

-q Quiet. This parameter minimizes screen output. It is useful when other device drivers (e.g. VGA BIOS) are present in the 28F020, and have been erased and not yet re-programmed.

The TC28F020.EXE program can be used to write one or more files to the Flash chip.

6.6.3 CONFIGURING THE TC486 FOR THE 28F020 DEVICE

The flash device should be installed in the IC15 socket on the TC486. Since this socket has been designed to accept a wide range of memory devices it will be necessary to configure the TC486 for the flash device as described in Appendix C.
6.6.4 PROGRAMMING A 29F040 DEVICE

The program which programs the 29F040 flash device is called TC29F040.EXE. It is run with the following parameters:

```
TC29F040 -ex -p<filename> -oxxxxx -lxxxxx -q
```

- **-e**: `-e` is used to specify which 64k block (1-8) of the device will be erased. If `x` is not specified the whole device will be erased. If `-e` is not specified the device will not be erased. The default is to not erase.

- **-p**: `-p<filename>` program the specified file into the device. This parameter defaults to "DO NOT PROGRAM".

- **-o**: `-oxxxxx` Start programming the file at this offset from the start of the flash device. `xxxx` is a 20 bit hexadecimal number. This parameter defaults to 0.

- **-l**: `-lxxxxx` This is the maximum amount of data to program into the flash EEPROM. The number of bytes programmed will be the either the file length or the number of bytes specified by this parameter whichever is the smaller. This parameter defaults to 3ffff bytes which is the size of the 28F040 device.

- **-q**: Quiet. This parameter minimizes screen output. It is useful when other device drivers (e.g. VGA BIOS) are present in the 28F040, and have been erased and not yet re-programmed.

The TC29F040.EXE program can be used to write one or more files to the Flash chip.

6.6.5 CONFIGURING THE TC486 FOR THE 29F040 DEVICE

The flash device should be installed in the IC15 socket on the TC486. Since this socket has been designed to accept a wide range of memory devices it will be necessary to configure the TC486 for the flash device as described in Appendix C.

6.6.6 USING THE FLASH CHIP AS A ROMDISK

The flash memory can be used as a ROM disk, either with or without an EPROM ROM disk.

A flash ROM disk is created in two stages: the disk image to go into the flash chip are generated as they would be for an EPROM ROM disk as described in section 6.3.2 and then the device is programmed as described in section 6.6.2.

A typical process is described below. There are clearly many options (one or two ROM disks, different drive letter allocations etc.) and so this example must be used as guidance for creating other variations.

The example described here is probably one of the most useful for practical applications. It allocates A: to an EPROM ROM disk and C: to a flash ROM disk. This partitioning allows users to use an EPROM for the BIOS, ROM disk driver and a ROM disk containing MS-DOS and other programs which do not need to be changed, and the flash ROM disk for programs and data which do need to be changed from time to time. The example shown here is for a 256k byte flash device. For other flash devices substitute the appropriate values into the MKDOSVOL utility command line parameters.

The first stage is to create the EPROM ROM disk. This is described in section 6.3.2. The EPROM ROM disk should be tested on its own (without a flash disk installed), to check that it has been programmed correctly.
The second stage is to create the flash ROM disk. This is initially very similar to the EPROM ROM disk process and is completed in two stages. Firstly a ROMdisk image is created as it would be for an EPROM ROM disk. Secondly this file is programmed into the flash device.

a Create a floppy (without DOS - format with the /U option ) and add programs and other files which you may later want to change. You could include a batch file (say FLASH.BAT) which is called from the AUTOEXEC.BAT batch file on the EPROM ROM disk to execute changeable programs on the flash disk.

b Create a binary image of the floppy by running MKDOSVOL. To make a 256k byte image to fill the 256k byte flash chip type:

MKDOSVOL MYIMAGE /K:100

e Program the resulting image file into the flash chip by typing:

TC28F020 -E -PMYIMAGE -O0

This assumes that the flash programming program (TC28F020.EXE) and the floppy image (MYIMAGE) are both on the same disk drive.

Test the flash ROM disk. You should see your files on the C: drive. There should be no need to re-boot the computer, since the ROM disk driver is already loaded and already expects C: to be present as a ROM disk.

You can change the flash ROM disk contents as often as you like, by repeating the second stage steps described above. Each time you must erase and reprogram the entire flash chip.

6.6.7 PROGRAMMING THE FLASH CHIP WITH FILES LOADED THROUGH THE SERIAL PORT

There is a useful technique available to allow the flash ROM disk to be re-programmed with files read across an RS-232 serial connection. Again, this is given here as an example, and users can adapt this example to suit their circumstances.

a Ensure that your CONFIG.SYS file has this entry:

```
DEVICE=INTERLNK.EXE
```

and ensure that INTERLNK.EXE is on your boot disk. (See the INTERLNK.DOC file in this directory for further information on INTERLNK).

b Ensure that TC28F020.EXE is available on your EPROM ROM disk (this is not absolutely essential, as it can be loaded from the remote computer using INTERLNK).

c When you need to update your flash ROM disk, prepare a replacement floppy image file using MKDOSVOL on a remote computer (e.g. desktop PC).

d Connect the TC486 to the remote PC with an RS-232 cable (a three-pin cable is sufficient: RxD, TxD and GND).

e Run INTERSVR on the remote PC. The remote PC becomes a server and its drives (and in particular the new flash ROM disk image) will be accessible from the TC486.

f Run INTERLNK on the TC486. This will map the remote PC’s drives to the TC486, so the TC386/486 can read files from the remote PC, via the serial port, as through they were on a local drive.

g Run the flash programming program to program the flash memory with a file on the remote PC. For example, if the new file is on the remote PC in a file C:\ROMDISK\NEWIMAGE, and if the remote C: is mapped as the local G: then type:
TC28F020 -E -PG:\ROMDISK\NEWIMAGE -O0

This will copy the file on the remote PC into the flash disk. When the down-loading is complete your TC486 will have a new ROM disk in its flash memory.
APPENDIX A: SPECIFICATION

Product: TC486

Description: PC/104 format, single board PC compatible computer.

Processor: TC386 - 80386SX running at 25Mhz.
TC486-25 - 80486SLC running at 25Mhz.
TC486-50 - 80486SLXC2 or 80486SLC2 internal clock speed of 50 MHz.

Memory: 0k, 512k, 1M, 2M or 4M DRAM.
Two sockets for byte-wide EPROM or RAM. To 1M bytes EPROM, 512K bytes SRAM, 512K bytes flash.
BIOS EPROM is 128k bytes as standard.

Printer port: Centronics compatible (PRN). Bidirectional.


Keyboard port: IBM AT compatible.

Mouse port: PS/2 compatible.

Speaker port: IBM AT compatible.

Reset circuit: Power supply monitor, PC/104 bus reset, watchdog timer and external reset switch capability.

Bus interface: PC/104 V2.2 16-bit

Interrupts: Standard PC and PC/AT interrupts are available on the PC/104 bus, (IRQ 9 [IRQ2], IRQ3 to IRQ6, IRQ10, IRQ11, IRQ14, IRQ15 and IOCHCK).

DMA: Standard PC and PC/AT DMA request and acknowledge pairs available on PC/104 bus. (DREQ 0 - 3, /DACK 0 - 3 and DREQ 5 - 7, /DACK 5 -7). Multiple bus masters (using the /MASTER signal) are not supported.


Dimensions: PCB - 3.550 inches * 3.775 inches, (91.7 mm * 95.8 mm Approx.). Overall dimensions including connectors, 3.9 inches * 4 inches, (99mm * 101.6mm Approx). Maximum height on the component side of the PCB is 11.5mm.

Weight: 95g Approx.

Operating temperature: 0 - 70 degrees C.

Humidity: 10% - 90% non-condensing.

Power Supplies: +5V at 660 mA - TC486-50 (4M byte DRAM)
+5V at 490 mA - TC486-25 (4M byte DRAM)
+5V at 410 mA - TC386-25 (4M byte DRAM)
APPENDIX B - DIFFERENCE BETWEEN REV B AND REV C TC486

This appendix details the changes between the Rev B and Rev C TC486. There are changes to the functionality as well as link settings and component / link positions. Users wishing to convert build instructions from the Rev B TC486 to the Rev C TC486 should read these notes carefully.

The Rev C TC486 has been designed so that current users of the Rev B TC486 can easily transfer over to the latest Rev C product with a minimum of fuss.

The component placement diagrams shown in Appendix D will be help in locating the various link positions discussed.

ENHANCEMENTS.

The Rev C TC486 is the same in functionally to the Rev B TC486 with the following enhancements.

- The capability of enabling or disabling COM1, COM2 or both serial ports using solder links.
- The COM2 serial port can be factory configured for RS485 operation.
- The parallel port can be enabled or disabled using solder links.
- The IRQ7 (printer port) interrupt request line can be made available to the PC/104 bus using solder links.
- A Eurom DiskOnChip and up to 1Mbyte EPROM/flash memory can be installed at the same time.
- Improved 1M byte memory mapping facility using solder links.

LINK SETTINGS - REV B - REV C CONVERSION

The Rev C TC486 has eight more link areas than the Rev B TC486 due to the added functionality of the Rev C board. In addition, some link areas have been replaced by others. The conversion notes below describe these changes.

<table>
<thead>
<tr>
<th>REV B</th>
<th>REV C</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>LK1</td>
<td>LK4</td>
<td>Function unchanged</td>
</tr>
<tr>
<td>LK2</td>
<td>LK3</td>
<td>Function unchanged</td>
</tr>
<tr>
<td>LK3</td>
<td>LK9</td>
<td>New function described below</td>
</tr>
<tr>
<td>LK4</td>
<td>LK5</td>
<td>Function unchanged</td>
</tr>
</tbody>
</table>

As can be seen LK1,2 & 4 have changed to LK4,3 & 5 respectively, however their function remains the same.

The Rev B LK3 link area has changed to LK9 on the Rev C TC486 and has also changed in functionality. This is to provide the necessary link options as described below.

LK9 IC12, 15 DEVICE SELECTION

Link 1-2  64k byte EPROM’s in IC12
Link 2-3  All other devices in IC12 (default setting)
Link 4-5  All other devices in IC15 (default setting)
Link 5-6  64k byte EPROM or Eurom DiskOnChip device in IC15
Although there are an additional eight link areas on the Rev C TC486 these do not affect conversion from the Rev B TC486. The eight additional link areas on the Rev C TC486 are configured as standard to provide the same functionality as the Rev B TC486. For information on how to change the additional link areas on the TC486 refer to Appendix C: TC486 REV C SETUP PROCEDURE.
APPENDIX C: TC486 SET-UP PROCEDURE - REV C TC486 ONLY.

A Rev C TC486 can be identified by the number printed on the component side of the PCB next to the J2 connector. A Rev C PCB will have the number ‘185001.C00’ printed on the PCB and a Rev B PCB will have the number ‘185001.B00’. See Appendix D: Component Placement diagrams for the location of the PCB revision number.

The set-up procedure described here should only be used with Rev C revision PCB’s.

The component placement diagram in Appendix D: may be of help in locating components referred to in this appendix.

BYTE WIDE MEMORY CONFIGURATION

The TC486 has two sockets for byte wide memory devices. IC12 can be an EPROM or FLASH device (it contains the bootstrap code and BIOS).

The link areas LK5, LK6 and LK9 are used to select the type of memory devices installed in the IC15 and IC12 sockets. IC12 can contain an EPROM or flash device, IC15 can contain an EPROM, an SRAM chip, a flash device or a Disk On Chip module.

IC12 - ALLOWABLE MEMORY DEVICES

- 64k byte EPROM e.g. 27C512
- 128k byte EPROM e.g. 27C1001
- 256k byte EPROM e.g. 27C2001
- 512k byte EPROM e.g. 27C4001
- 1M byte EPROM e.g. 27C8001
- 256k or 512k byte Flash chip

IC15 - ALLOWABLE MEMORY DEVICES

- No memory chip
- 128k or 512K byte Static RAM
- 128k, 256k, 512k or 1M byte EPROM
- Eurom DiskOnChip
- 256k or 512k byte Flash chip

DRAM CONFIGURATION

The standard TC486 product is delivered with no DRAM fitted as standard. Various DRAM configurations are possible. See section 2.3 - DRAM. The TC486 has been designed for zig-zag style DRAMs. A maximum of eight of these devices can be installed on the TC486. These are numbered IC1 to IC8 on the PCB. Users may buy DRAM from DSP Design or fit their own (see section 2.3 for notes on DRAM speed).
SOLDER LINK AREAS - REV C TC486 ONLY

A number of functions can be configured with solder links on the back of the TC486 board. The board layout is so dense we have implemented these configuration options with solder links which take less space than jumpers as well as being more reliable.

Care must be taken when changing these link areas so that no accidental shorts are produced or created.

**LK1 MEMORY MAPPING OF ADDRESS REGION D0000H-DFFFFH.**

LK1 is a 3*1 solder link area and is linked 2-3 as standard.

- **LK1: 1-2** D0000H-DFFFFH is mapped offboard.
- **LK1: 2-3** D0000H-DFFFFH is mapped to the IC15 socket.

**LK2 MEMORY MAPPING OF ADDRESS REGION E0000H-EFFFFH.**

LK2 is a 3*1 solder link area and is linked 2-3 as standard.

- **LK2: 1-2** E0000H-EFFFFH is mapped offboard.
- **LK2: 2-3** E000H-EFFFFH is mapped to the IC15 socket.

**LK3 IC15 BATTERY BACKUP**

LK3 is located on the rear of the PCB, near pin 20 of IC8 (DRAM). It is a 3*1 solder link area. Standard configuration is linked 1-2.

- **Link 1-2** Enables battery backup of SRAM chip in IC15.
- **Link 2-3** For non-battery backed use.

**LK4 IC15 BATTERY BACKUP**

LK4 is located on the rear of the PCB, near to pin 50 of the J3 I/O connector. It is a 3*1 solder link area. Standard configuration is linked 1-2. Only SRAM chips can be battery backed. Do not attempt to battery backup EPROM or flash chips.

- **Link 1-2** Enables battery backup of SRAM chip in IC15.
- **Link 2-3** For non-battery backed use.

**LK5 IC15 DEVICE AND SIZE SELECTION**

LK5 is located on the rear and in the centre of the PCB. It is a 4*2 solder link area. Standard configuration is linked 1-2, 4-5 and 7-8. Link as follows:

- **SRAM**
  - 128k & 512k bytes LK5: 1-2, 4-5, 7-8

- **EPROM**
  - 128k byte LK5: 5-6, 2-3, 1-8
  - 256k byte LK5: 5-6, 2-3, 1-8
  - 512k byte LK5: 5-6, 2-3, 1-8
  - 1M byte LK5: 4-5, 2-3, 1-8

- **FLASH**
  - 128k byte LK5: 5-6, 2-7, 1-8
  - 256k LK5: 5-6, 2-7, 1-8
**EUROM DiskOnChip**  LK5: 1-8, 2-7, 5-6

**LK6**  **FACTORY FITTED**

This link area is set at the factory and should not be altered.

**LK7**  **COM2 RS232 ENABLE / DISABLE**

LK7 is a 3*1 solder link area and is linked 1-2 (enabled) as standard.

<table>
<thead>
<tr>
<th>Link</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>LK7: 1-2</td>
<td>COM2: RS232 serial port is enabled.</td>
</tr>
<tr>
<td>LK7: 2-3</td>
<td>COM2: RS232 serial port is disabled.</td>
</tr>
</tbody>
</table>

**LK8**  **INTERNUPT IRQ7 ALLOCATION.**

LK8 is a 3*1 solder link area and is fitted as standard.

<table>
<thead>
<tr>
<th>Link</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>LK8: Fit</td>
<td>Printer drives IRQ7.</td>
</tr>
<tr>
<td>LK8: Omit</td>
<td>IRQ7 is available for PC/104 bus interrupts.</td>
</tr>
</tbody>
</table>

**LK9**  **IC12 & IC15 DEVICE SIZE SELECTION**

LK9 is located on the rear and in the centre of the PCB. It is a 3*1 solder link area. Standard configuration is linked 2-3 and 4-5.

<table>
<thead>
<tr>
<th>Link</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Link: 1-2</td>
<td>64k byte EPROM's.</td>
</tr>
<tr>
<td>Link: 2-3</td>
<td>All other devices in IC12.</td>
</tr>
<tr>
<td>Link 5-6</td>
<td>64k byte EPROM or Eurom TC1102 DiskOnChip in IC15 socket.</td>
</tr>
<tr>
<td>Link 4-5</td>
<td>All other devices in IC15.</td>
</tr>
</tbody>
</table>

**LK10**  **COM1 SERIAL PORT ENABLE / DISABLE**

LK10 is a 3*1 solder link area and is linked 2-3 (enabled) as standard.

<table>
<thead>
<tr>
<th>Link</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>LK10: 1-2</td>
<td>COM1: Serial port is disabled.</td>
</tr>
<tr>
<td>LK10: 2-3</td>
<td>COM1: Serial port is enabled.</td>
</tr>
</tbody>
</table>

**LK11**  **PRINTER PORT ENABLE / DISABLE**

LK11 is a 3*1 solder link area and is linked 1-2 (enabled) as standard.

<table>
<thead>
<tr>
<th>Link</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>LK11: 1-2</td>
<td>Printer port is enabled.</td>
</tr>
<tr>
<td>LK11: 2-3</td>
<td>Printer port is disabled.</td>
</tr>
</tbody>
</table>

**LK12**  **COM2 SERIAL PORT ENABLE / DISABLE**

LK12 is a 3*1 solder link area and is linked 1-2 (enabled) as standard.

<table>
<thead>
<tr>
<th>Link</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>LK12: 1-2</td>
<td>COM2: Serial port is enabled.</td>
</tr>
<tr>
<td>LK12: 2-3</td>
<td>COM2: Serial port is disabled.</td>
</tr>
</tbody>
</table>
**TC486 SET-UP PROCEDURE - REV B TC486 ONLY**

A Rev B TC486 can be identified by the number printed on the component side of the PCB next to the J2 connector. A Rev B PCB will have the number ‘185001.B00’ printed on the PCB and a Rev C PCB will have the number ‘185001.C00’. The set-up procedure described here should only be used with Rev B revision PCB’s.

The set-up procedure described here should only be used with Rev B revision PCB’s.

The component placement diagram in Appendix D: may be of help in locating components referred to in this appendix.

**BYTE WIDE MEMORY CONFIGURATION**

The TC486 has two sockets for byte wide memory devices. IC12 is always an EPROM (it contains the bootstrap code and BIOS).

The link areas LK1 and LK4 are used to select the type of memory devices installed in the IC15 and IC12 sockets. IC12 contains EPROM, IC15 can contain an EPROM, an SRAM chip, a flash device or a EUROM DiskOnChip module.

### IC12 - ALLOWABLE MEMORY DEVICES

- 64k byte EPROM e.g. 27C512
- 128k byte EPROM e.g. 27C1001
- 256k byte EPROM e.g. 27C2001
- 512k byte EPROM e.g. 27C4001
- 1M bytes EPROM e.g. 27C8001

### IC15 - ALLOWABLE MEMORY DEVICES

- No memory chip
- 128k or 512K byte Static RAM
- 128k, 256k, 512k or 1M byte EPROM
- Eurom DiskOnChip
- 256k or 512k byte Flash chip

**DRAM CONFIGURATION**

The standard TC486 product is delivered with no DRAM fitted as standard. Various DRAM configurations are possible. See section 2.3 - DRAM. The TC486 has been designed for zig-zag style DRAMs. A maximum of eight of these devices can be installed on the TC486. These are numbered IC1 to IC8 on the PCB.

Users may buy DRAM from DSP Design or fit their own (see section 2.3 for notes on DRAM speed).
SOLDER LINK AREAS - REV B PCB ONLY

A number of functions can be configured with solder links on the back of the TC486 board. The board layout is so dense we have implemented these configuration options with solder links which take less space than jumpers as well as being more reliable.

Care must be taken when changing these link areas so that no solder is allowed to short any pins that should not be shorted.

LK1  IC15 BATTERY BACKUP

LK1 is located on the rear of the PCB, near pin 50 of the J3 I/O connector. It is a 3*1 solder link area. Standard configuration is linked 1-2. Only SRAM chips can be battery backed. Do not attempt to battery backup EPROM or flash chips.

- Link 1-2 enables battery backup of SRAM chip in IC15.
- Link 2-3 for non-battery backed use.

LK2  IC15 BATTERY BACKUP

LK3 is located on the rear of the PCB, near pin 20 of IC8 (DRAM). It is a 3*1 solder link area. Standard configuration is linked 1-2.

- Link 1-2 enables battery backup of SRAM chip in IC15.
- Link 2-3 for non-battery backed use.

LK3  IC12 DEVICE SIZE SELECTION

LK3 is located on the rear and in the centre of the PCB. It is a 3*1 solder link area. Standard configuration is linked 2-3.

- Link: 1-2 64k byte EPROM's.
- Link: 2-3 All other devices in IC12. (default)

LK4  IC15 DEVICE AND SIZE SELECTION

LK4 is located on the rear and in the centre of the PCB. It is a 4*2 solder link area. Standard configuration is linked 1-2, 4-5 and 7-8. Link as follows:

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Size</th>
<th>Link Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRAM</td>
<td>128k</td>
<td>1-2, 4-5, 7-8</td>
</tr>
<tr>
<td></td>
<td>512k</td>
<td>LK5</td>
</tr>
<tr>
<td>EPROM</td>
<td>128k</td>
<td>Link: 5-6, 2-3, 1-8</td>
</tr>
<tr>
<td></td>
<td>256k</td>
<td>Link: 5-6, 2-3, 1-8</td>
</tr>
<tr>
<td></td>
<td>512k</td>
<td>Link: 5-6, 2-3, 1-8</td>
</tr>
<tr>
<td></td>
<td>1M</td>
<td>Link: 4-5, 2-3, 1-8</td>
</tr>
<tr>
<td>FLASH</td>
<td>128k</td>
<td>Link: 5-6, 2-7, 1-8</td>
</tr>
<tr>
<td></td>
<td>256k</td>
<td>Link: 5-6, 2-7, 1-8</td>
</tr>
<tr>
<td></td>
<td>512k (28F4001)</td>
<td>Link: 5-6, 2-3, 1-8</td>
</tr>
<tr>
<td></td>
<td>512k (29F040)</td>
<td>Link: 4-5, 2-7, 1-8</td>
</tr>
<tr>
<td>EUROM DISK ON CHIP</td>
<td>Link:</td>
<td>1-8, 2-7, 5-6</td>
</tr>
</tbody>
</table>

Note: If a DiskOnChip module is to be fitted in the IC15 position then LK3 needs to be linked 1-2 and 2-3. In this case IC12 must be a 64K byte or 128K byte EPROM.
DRAM INSTALLATION INSTRUCTIONS

The following instructions assume a standard TC486 board with no DRAM installed.

All anti-static precautions must be observed when handling static sensitive devices. Failure to do so may result in damage and subsequent failure of the TC486.

Suitable DRAM devices are available from DSP Design as standard parts. See Appendix D - options and ordering information.

512K OPTION

The 512k DRAM option is the minimum DRAM configuration available and requires four (256 * 4) zig-zag DRAM devices. These are to be installed in positions IC5, IC6, IC7 & IC8. Pin 1 of each device must line up with the pin 1 ident on the PCB.

1M byte OPTION

The 1M byte option requires eight of the (256*4) zig-zag DRAM devices. These are to be installed in positions IC1 to IC8 inclusive. Pin 1 of each device must line up with the pin 1 ident on the PCB. This option is the maximum available configuration using (256*4) DRAM devices.

2M byte OPTION

The 2M byte option requires four of the (1M*4) zig-zag DRAM devices. These should be installed in the IC5 to IC8 positions. Pin 1 of each device must line up with the pin 1 ident on the PCB.

4M byte OPTION

The 4M byte option is the maximum configuration that is currently available on the TC486. This option requires eight of the (1M*4) zig-zag DRAM devices which should be installed in the IC1 to IC8 positions. Pin 1 of each device must line up with the pin 1 ident on the PCB.

NOTE: It may be possible to increase the maximum DRAM configuration beyond 4M byte with a plug in daughter board.
APPENDIX D: COMPONENT PLACEMENT DIAGRAMS

The two component placement diagrams which follow (one for each side of the TC486) may be of help in locating the components referred to in Appendix B.
REV B TC486 COMPONENT PLACEMENT DIAGRAMS
APPENDIX E: TC486 OPTIONS AND ORDERING INFORMATION

The standard TC486 is fitted with 0M bytes of DRAM, two serial ports, Centronics port, sound port, keyboard interface, mouse interface and BIOS EPROM. Options which can be added to the base unit are detailed below.

**Base Unit**
- TC386: 80386SX based processor board.
- TC486-25: 486SLC based processor board.
- TC486-50: 486SLC2 based processor board.
- TC386-T25: TC386 with stackthrough connectors as standard.
- TC486-T50: TC486-50 with stackthrough connectors as standard.

**DRAM**
- ZD512: DRAM 512k bytes (contains four 256 x 4 zig-zag DRAM chips)
- ZD1: DRAM 1M bytes (contains eight 256 x 4 zig-zag DRAM chips)
- ZD2: DRAM 2M bytes (contains four 1M x 4 zig-zag DRAM chips)
- ZD4: DRAM 4M bytes (contains eight 1M x 4 zig-zag DRAM chips)

**ACCESSORIES**

The following part numbers should be used to order various accessories:
- TCDEV: PC/104 Development Platform
- TCDOS: Microsoft MS-DOS Operating System
- TCWIN: Windows operating system
- TCUTILS: Utilities disk including ROM disk generation program and RAM disk driver
- TCPSU: Power supply unit for the TCDEV
- TRM-TC: Technical reference manual
- TCDISK-420: IDE drive for the TCDEV
- BAT32D: 32 pin battery back-up socket
-EPROM128: 128k byte EPROM
-EPROM256: 256k byte EPROM
-EPROM512: 512k byte EPROM
- RAM128: 128k byte SRAM
- TCPAK: Contains a TCDEV, TCPSU, TCUTILS AND TRM-TC in one starter pack
- TC1102-D01: 1M byte Eurom Disk On Chip module configured for TC processor cards
- TC1102-D02: 2M byte Eurom Disk On Chip module configured for TC processor cards
- IDE3020: Cable to convert 2.5inch IDE connector to 3.5 inch IDE connector and vica-versa

**PC/104 MODULES**

The following list describes various cards that are available from DSP Design. Contact your supplier for a more comprehensive list.

**FLASH DISKS**
- TFD-01: 1M byte PC/104 flash disk module
- TFD-02: 2M byte PC/104 flash disk module
- TFD-04: 4M byte PC/104 flash disk module
- TFD-08: 8M byte PC/104 flash disk module
- TFD-010: 10M byte PC/104 flash disk module
- TFD-016: 16M byte PC/104 flash disk module
- TFD-032: 32M byte PC/104 flash disk module

**I/O modules**
DSP Design have designed a number of PC/104 boards specifically for the PC/104 bus. Contact your supplier for more details.

<table>
<thead>
<tr>
<th>Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSYST</td>
<td>System I/O board, comprising serial ports, parallel port, floppy &amp; hard disk drive controller</td>
</tr>
<tr>
<td>TCMCIA-2</td>
<td>Two slot PCMCIA interface card.</td>
</tr>
<tr>
<td>TPO24</td>
<td>Opto-isolated I/O board. Twelve inputs and twelve outputs</td>
</tr>
<tr>
<td>TP406</td>
<td>Parallel I/O and timer board. Forty lines of parallel I/O</td>
</tr>
<tr>
<td>TENET</td>
<td>Ethernet interface card</td>
</tr>
<tr>
<td>TCSCSI12-16</td>
<td>16-bit SCSI interface card</td>
</tr>
<tr>
<td>TS400</td>
<td>Four serial interfaces on one card</td>
</tr>
<tr>
<td>TAD12</td>
<td>12-bit Analogue to Digital converter card</td>
</tr>
</tbody>
</table>
APPENDIX F: CABLE PIN ASSIGNMENTS

TC486 PERIPHERAL CONNECTORS

The peripheral devices are connected to the TC486 through a 50 way IDC connector, called J3. The 50 pins on the connector are brought to the outside world through a 50 way 0.1 inch IDC right angled connector.

The table E1 which follows lists the J3 signal name and also the peripheral to which the signal belongs and the pin number of that peripheral's connector. The standard connectors used in PC's for each of the peripherals are:

- Centronics Printer: 25 way female D-type
- Keyboard: 5 way female circular DIN
- Mouse: 6 pin mini DIN (PS/2 style)
- Serial COM1: 9 way D-type
- Serial COM2: 9 way male D-type
- Loudspeaker: N/A
- Battery: N/A
- Reset Switch: N/A

<table>
<thead>
<tr>
<th>J3 PIN</th>
<th>SIGNAL</th>
<th>PERIPHERAL</th>
<th>PIN</th>
<th>J3 PIN</th>
<th>SIGNAL</th>
<th>PERIPHERAL</th>
<th>PIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
<td>MOUSE</td>
<td>3</td>
<td>2</td>
<td>VCC</td>
<td>MOUSE</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>MCLOCK</td>
<td>MOUSE</td>
<td>5</td>
<td>4</td>
<td>MDATA</td>
<td>MOUSE</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>SLCT</td>
<td>CENTRONICS</td>
<td>13</td>
<td>6</td>
<td>PE</td>
<td>CENTRONICS</td>
<td>12</td>
</tr>
<tr>
<td>7</td>
<td>BUSY</td>
<td>CENTRONICS</td>
<td>11</td>
<td>8</td>
<td>/ACK</td>
<td>CENTRONICS</td>
<td>10</td>
</tr>
<tr>
<td>9</td>
<td>PD7</td>
<td>CENTRONICS</td>
<td>9</td>
<td>10</td>
<td>PD6</td>
<td>CENTRONICS</td>
<td>8</td>
</tr>
<tr>
<td>11</td>
<td>PD5</td>
<td>CENTRONICS</td>
<td>7</td>
<td>12</td>
<td>PD4</td>
<td>CENTRONICS</td>
<td>6</td>
</tr>
<tr>
<td>13</td>
<td>GND</td>
<td>CENTRONICS</td>
<td>*</td>
<td>14</td>
<td>PD3</td>
<td>CENTRONICS</td>
<td>5</td>
</tr>
<tr>
<td>15</td>
<td>/SLCTIN</td>
<td>CENTRONICS</td>
<td>17</td>
<td>16</td>
<td>PD2</td>
<td>CENTRONICS</td>
<td>4</td>
</tr>
<tr>
<td>17</td>
<td>/INIT</td>
<td>CENTRONICS</td>
<td>16</td>
<td>18</td>
<td>PD1</td>
<td>CENTRONICS</td>
<td>3</td>
</tr>
<tr>
<td>19</td>
<td>/ERROR</td>
<td>CENTRONICS</td>
<td>15</td>
<td>20</td>
<td>PD0</td>
<td>CENTRONICS</td>
<td>2</td>
</tr>
<tr>
<td>21</td>
<td>/AUTOFD</td>
<td>CENTRONICS</td>
<td>14</td>
<td>22</td>
<td>/STROBE</td>
<td>CENTRONICS</td>
<td>1</td>
</tr>
<tr>
<td>23</td>
<td>GND</td>
<td>RESET SWITCH</td>
<td>24</td>
<td></td>
<td>/RESET</td>
<td>RESET SWITCH</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>VCC</td>
<td>SPEAKER</td>
<td>26</td>
<td></td>
<td>SPKR</td>
<td>SPEAKER</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>GND</td>
<td>BATTERY</td>
<td>-</td>
<td>28</td>
<td>BATT</td>
<td>BATTERY</td>
<td>-</td>
</tr>
<tr>
<td>29</td>
<td>VCC</td>
<td>KEYBOARD</td>
<td>5</td>
<td>30</td>
<td>/KBDATA</td>
<td>KEYBOARD</td>
<td>2</td>
</tr>
<tr>
<td>31</td>
<td>GND</td>
<td>KEYBOARD</td>
<td>4</td>
<td>32</td>
<td>/KBCLK</td>
<td>KEYBOARD</td>
<td>1</td>
</tr>
<tr>
<td>33</td>
<td>GND</td>
<td>COM2</td>
<td>5</td>
<td>34</td>
<td>RI1</td>
<td>COM2</td>
<td>9</td>
</tr>
<tr>
<td>35</td>
<td>DTR1</td>
<td>COM2</td>
<td>4</td>
<td>36</td>
<td>CTS1</td>
<td>COM2</td>
<td>8</td>
</tr>
<tr>
<td>37</td>
<td>TXD1</td>
<td>COM2</td>
<td>3</td>
<td>38</td>
<td>RTS1</td>
<td>COM2</td>
<td>7</td>
</tr>
<tr>
<td>39</td>
<td>RXD1</td>
<td>COM2</td>
<td>2</td>
<td>40</td>
<td>DSR1</td>
<td>COM2</td>
<td>6</td>
</tr>
<tr>
<td>41</td>
<td>DCD1</td>
<td>COM2</td>
<td>1</td>
<td>42</td>
<td>GND</td>
<td>COM1</td>
<td>5</td>
</tr>
<tr>
<td>43</td>
<td>R10</td>
<td>COM1</td>
<td>9</td>
<td>44</td>
<td>DTR0</td>
<td>COM1</td>
<td>4</td>
</tr>
<tr>
<td>45</td>
<td>CTS0</td>
<td>COM1</td>
<td>8</td>
<td>46</td>
<td>TXD0</td>
<td>COM1</td>
<td>3</td>
</tr>
<tr>
<td>47</td>
<td>RTS0</td>
<td>COM1</td>
<td>7</td>
<td>48</td>
<td>RXD0</td>
<td>COM1</td>
<td>2</td>
</tr>
<tr>
<td>49</td>
<td>DSR0</td>
<td>COM1</td>
<td>6</td>
<td>50</td>
<td>DCD0</td>
<td>COM1</td>
<td>1</td>
</tr>
</tbody>
</table>

*NOTE: J3 PIN 13 Connects to CENTRONICS PORT pins 18 to 25 inclusive.

TABLE  6: J3 I/O CONNECTOR PIN ASSIGNMENTS

Pin 1 of the J3 connector can be identified by looking at the J3 ident on the TC486. The J3 connector is surrounded by a box and in one corner of the box is a small solid square. This denotes pin 1 of the J3 I/O connector. All odd numbered pins are in one row and all even numbered pins are in the other row.

J4 POWER CONNECTOR
The J4 connector is used to provide an alternate power inlet to the TC486 for stand alone operation. The J4 connector uses industry standard parts and a number of manufacturers are able to provide suitable mating halves.

The J4 connector used on the TC486 is a MOLEX mini KK, 2.5mm pitch, 5046 series right angled header with friction lock. A suitable mating half would be the MOLEX mini KK 2.5mm pitch 5051 series crimp polarizing housing. Crimp pins are required for this housing connector and these are also available from MOLEX. At the time of writing FARNELL ELECTRONIC SERVICES supply these MOLEX parts as standard with the stock numbers 011007D for the polarized housing connector and 011122R for the crimp pins.

<table>
<thead>
<tr>
<th>J4 PIN</th>
<th>SIGNAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>+5V</td>
</tr>
<tr>
<td>4</td>
<td>+5V</td>
</tr>
</tbody>
</table>

TABLE 7: J4 POWER CONNECTOR PIN ASSIGNMENTS

Pin 1 of the J4 connector can be identified by looking at the silk-screen ident on the TC486 PCB. Pin 1 has a ‘1’ to the right hand side of the connector.
BUS CONNECTORS

The PC/104 bus connector pin assignments conform to the PC/104 bus specification V2.2. The pin assignment is shown below.

<table>
<thead>
<tr>
<th>PIN</th>
<th>J1 ROW A</th>
<th>J1 ROW B</th>
<th>PIN</th>
<th>J2 ROW C</th>
<th>J2 ROW D</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>-</td>
<td>-</td>
<td>0</td>
<td>0V</td>
<td>0V</td>
</tr>
<tr>
<td>1</td>
<td>/IOCHCHK</td>
<td>0V</td>
<td>1</td>
<td>/SBHE</td>
<td>/MEMCS16</td>
</tr>
<tr>
<td>2</td>
<td>SD7</td>
<td>RESETDRV</td>
<td>2</td>
<td>LA23</td>
<td>/IOCS16</td>
</tr>
<tr>
<td>3</td>
<td>SD6</td>
<td>+5V</td>
<td>3</td>
<td>LA22</td>
<td>IRQ10</td>
</tr>
<tr>
<td>4</td>
<td>SD5</td>
<td>IRQ9</td>
<td>4</td>
<td>LA21</td>
<td>IRQ11</td>
</tr>
<tr>
<td>5</td>
<td>SD4</td>
<td>-5V*</td>
<td>5</td>
<td>LA20</td>
<td>IRQ12</td>
</tr>
<tr>
<td>6</td>
<td>SD3</td>
<td>DRQ2</td>
<td>6</td>
<td>LA19</td>
<td>IRQ15</td>
</tr>
<tr>
<td>7</td>
<td>SD2</td>
<td>-12V*</td>
<td>7</td>
<td>LA18</td>
<td>IRQ14</td>
</tr>
<tr>
<td>8</td>
<td>SD1</td>
<td>/EN DXFR</td>
<td>8</td>
<td>LA17</td>
<td>/DACK0</td>
</tr>
<tr>
<td>9</td>
<td>SD0</td>
<td>+12V*</td>
<td>9</td>
<td>/MEMR</td>
<td>DREQ0</td>
</tr>
<tr>
<td>10</td>
<td>IOCHR RDY</td>
<td>(KEY)</td>
<td>10</td>
<td>/MEMW</td>
<td>/DACK5</td>
</tr>
<tr>
<td>11</td>
<td>AEN</td>
<td>/SMEMW</td>
<td>11</td>
<td>SD8</td>
<td>DRQ5</td>
</tr>
<tr>
<td>12</td>
<td>SA19</td>
<td>/SMEMR</td>
<td>12</td>
<td>SD9</td>
<td>/DACK6</td>
</tr>
<tr>
<td>13</td>
<td>SA18</td>
<td>/IO W</td>
<td>13</td>
<td>SD10</td>
<td>DRQ6</td>
</tr>
<tr>
<td>14</td>
<td>SA17</td>
<td>/IOR</td>
<td>14</td>
<td>SD11</td>
<td>/DACK7</td>
</tr>
<tr>
<td>15</td>
<td>SA16</td>
<td>/DACK3</td>
<td>15</td>
<td>SD12</td>
<td>DRQ7</td>
</tr>
<tr>
<td>16</td>
<td>SA15</td>
<td>DRQ3</td>
<td>16</td>
<td>SD13</td>
<td>+5V</td>
</tr>
<tr>
<td>17</td>
<td>SA14</td>
<td>/DACK1</td>
<td>17</td>
<td>SD14</td>
<td>/MASTER*</td>
</tr>
<tr>
<td>18</td>
<td>SA13</td>
<td>DRQ1</td>
<td>18</td>
<td>SD15</td>
<td>0V</td>
</tr>
<tr>
<td>19</td>
<td>SA12</td>
<td>/REFRESH</td>
<td>19</td>
<td>(KEY)</td>
<td>0V</td>
</tr>
<tr>
<td>20</td>
<td>SA11</td>
<td>SYSCLK</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>SA10</td>
<td>IRQ7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>SA9</td>
<td>IRQ6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>SA8</td>
<td>IRQ5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>SA7</td>
<td>IRQ4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>SA6</td>
<td>IRQ3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>SA5</td>
<td>/DACK2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>SA4</td>
<td>TC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>SA3</td>
<td>BALE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>SA2</td>
<td>+5V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>SA1</td>
<td>OSC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>SA0</td>
<td>0V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>0V</td>
<td>0V</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* NOTE: These connections are not implemented on the TC486.

TABLE 8: PC/104 PIN ASSIGNMENTSPin 1 of J1 connector is marked on the PCB silk-screen with a '1', rows A and B are also marked. J2 pin 0 and Rows C & D are identified in the same way.
APPENDIX G: POWER REDUCTION OPTIONS

The SCATsx register index 46H provides some power management functions that enable you to reduce power consumption. This essentially consists of slowing the processor clock speed hence reducing the power required by the processor and memory. You are able to further reduce power consumption by enabling sleep mode and causing the processor to execute a HALT instruction. When halted the processor is not able to perform any program execution and will remain in this mode until receipt of an interrupt. If sleep mode is enabled, the SCATsx detects the HALT opcode and responds by reducing the processor clock speed automatically. Both of these options are discussed below.

CHANING THE PROCESSOR SPEED.

Index register 46H allows the processor clock speed to be changed. The processor speed can be reduced by a factor of 2, 4 or 8. Bits 2 and 3 of index register 46H should be set as indicated in the table below to select the desired frequency of the processor clock. All other bits should remain the same.

<table>
<thead>
<tr>
<th>BIT 3 - 2</th>
<th>PROCESSOR CLOCK</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 - 0</td>
<td>Processor clock running at full speed (Default on reset).</td>
</tr>
<tr>
<td>0 - 1</td>
<td>Processor clock divided by 2.</td>
</tr>
<tr>
<td>1 - 0</td>
<td>Processor clock divided by 4.</td>
</tr>
<tr>
<td>1 - 1</td>
<td>Processor clock divided by 8.</td>
</tr>
</tbody>
</table>

TABLE 9: ICR 46H PROCESSOR SPEED CONTROL

The standard BIOS for the TC486 (185010.B**) after reset has an index register 46H value of 43H. From the table above we can see that the value 43H corresponds to a processor clock running at full speed. To reduce the processor clock to say one eighth of its maximum frequency, set index 46H to the value 4FH.

Index register 46H is accessed by first writing ‘46H’ to I/O port 22H. This is followed by an I/O read at port 23H to read the current value or an I/O write to set a new value.

Example of reducing the processor clock to one eighth of its maximum run frequency, using DOS's DEBUG program:

O22,46
O23,4F

The following assembler code does the same as the above example:

```
MOV AL, 46H ; Index 46H
OUT 22H, AL ; Output to index register
JMP $+2 ;
IN AL, 23H ; Read current value
JMP $+2 ;
OR AL, 0CH ; Set bits 2 and 3
OUT 23H, AL
```
SLEEP MODE

The processor can be halted by executing the HALT instruction. It will then stop executing instructions. When an interrupt (IRQ) or NMI is generated the processor will continue execution with the instruction after the HALT.

The processor can only be put into sleep mode by executing a HALT instruction when sleep mode is enabled. In sleep mode the processor clock frequency is automatically reduced. The combination of reduced processor speed and suspension of instruction execution provides lower power operation.

Sleep mode is disabled by reset. To enable sleep mode bit 7 of SCATsx internal configuration register (ICR) 46H must be set. Bits 0 and 1 of this register must be set to 1 also to select a minimum clock frequency for sleep mode.

Once sleep mode has been enabled the processor can enter sleep mode by executing a HALT instruction. It will remain halted with a reduced processor clock frequency until an interrupt (INTR or NMI) is detected. A DMA or on board refresh cycle will terminate sleep mode temporarily. The processor will return to sleep mode upon completion of the DMA or refresh.

You can include HALT instructions in your application program to enter lower power modes whilst waiting for interrupts. Note in the absence of other interrupts the DOS timer tick will normally generate interrupts at 18.2Hz.

Sleep mode can be enabled by using the DOS DEBUG.EXE program. Type the following commands at the debug '-' prompt:

O22,46
O23,C3
Q

The following assembler code extract also will enable sleep mode:

```
MOV AL, 46H ; Index 46H
OUT 22H, AL ; Output to index register
JMP $+2 ;
IN AL, 23H ; Read current value
JMP $+2 ;
OR AL, 83H ; Set bits 0 and 1
OUT 23H, AL
```

When sleep mode is enabled you can explore sleep mode operation with the following assembler code extract:

```
MOV CX,100H ; Loop counter
HALT_AGAIN: HALT ; Halt and wait for DOS timer tick interrupt
DEC CX ; Decrement counter
JNZ HALT_AGAIN ; If counter not zero do again
NOP ; Terminates here when loop counter expires
       ; roughly 256/18 seconds.
```

Table 10 shows comparative power consumption figures for differing processor clock speeds assuming 4M byte of DRAM is installed and the standard BIOS (185010.B01) is fitted. The processor performance for each setting is indicated by the Norton SI rating in parenthesis.

<table>
<thead>
<tr>
<th>PROCESSOR</th>
<th>CLK</th>
<th>CLK/2 (SI)</th>
<th>CLK/4 (SI)</th>
<th>CLK/8 (SI)</th>
<th>SLEEP+HALT</th>
</tr>
</thead>
<tbody>
<tr>
<td>TC486-50</td>
<td>660mA (89)</td>
<td>555mA (43)</td>
<td>444mA (21)</td>
<td>358mA (12)</td>
<td>166mA</td>
</tr>
<tr>
<td></td>
<td>TC486-25</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>----------------</td>
<td>----------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
</tr>
<tr>
<td></td>
<td>490mA</td>
<td>400mA</td>
<td>344mA</td>
<td>315mA</td>
<td>135mA</td>
</tr>
<tr>
<td></td>
<td>(49)</td>
<td>(24)</td>
<td>(14)</td>
<td>(7)</td>
<td></td>
</tr>
<tr>
<td>TC386</td>
<td>410mA</td>
<td>330mA</td>
<td>270mA</td>
<td>245mA</td>
<td>200mA</td>
</tr>
<tr>
<td></td>
<td>(23)</td>
<td>(11)</td>
<td>(7)</td>
<td>(3.5)</td>
<td></td>
</tr>
<tr>
<td>ICR 46H value</td>
<td>43H</td>
<td>47H</td>
<td>4BH</td>
<td>4FH</td>
<td>C3H</td>
</tr>
</tbody>
</table>

TABLE 10: CURRENT CONSUMPTION AT VARYING PROCESSOR SPEEDS
APPENDIX H: FAULT REPORTING

DSP Design makes every effort to ship products and documentation which are completely free from faults, design errors and inconsistencies. Sometimes, however, problems do show up in the field. To help us put these right as quickly and efficiently as possible, we need as much information as possible from you, the user.

For this reason we have included here a “Product Fault Report” form. If you ever have cause to return a board for repair, or if you detect an error in the documentation, we would appreciate it if you could fill in the form on the next page, or a copy of it, and return the form to your supplier.

Prior to returning a faulty product, please check the following:

1. The board has been correctly configured for the intended application (see earlier appendix for board installation details).
2. The power supplies are providing correct voltage levels.
3. Cabling to the board is sound and connected correctly.
4. Other cards in the system are known to be correctly configured and functioning.
5. **PLEASE RETURN THE BOARD TO US IN EXACTLY THE SAME CONFIGURATION AS IT FAILED IN.**

Your help with this will enable us to sort out your problem more quickly. Thank you.
PRODUCT FAULT REPORT

CUSTOMER INFORMATION
COMPANY NAME:
INDIVIDUAL CONTACT:
PHONE NO:

PRODUCT INFORMATION
PRODUCT/DOCUMENT:
SERIAL NO:
DATE OF RETURN:

SYMPTOMS OBSERVED /DOCUMENTATION ERRORS (as applicable):

IN WHAT CONFIGURATION IS THE BOARD USUALLY USED? (WHAT OTHER BOARDS, WHAT SOFTWARE ETC.)?

FOR DSP DESIGN USE ONLY:

PRODUCT TEST REPORT:

DATE OF RECEIPT: REPAIRED BY:
CHARGES TO BE INVOICED: £
DATE OF RETURN: RETURNED BY: